BASIC ELECTRONICS ENGINEERING

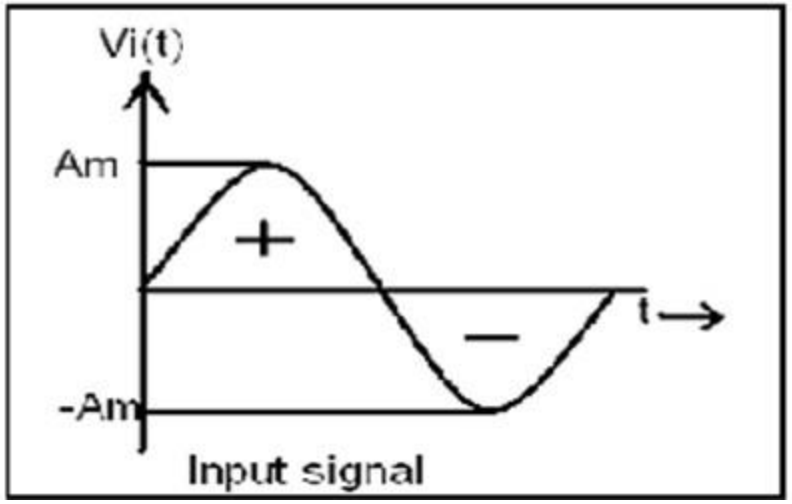
(RBL1B002)

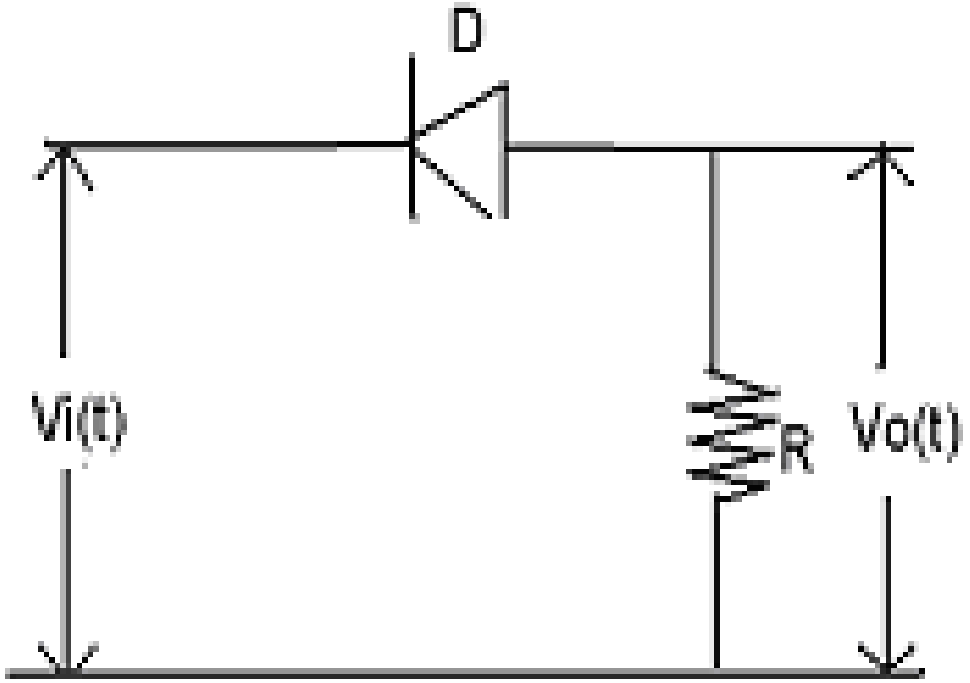
MODULE-1

Clipper Circuits

- The circuit can remove or clip a certain portion of the input signal above / below a specified level is called as Clipper Circuits.
- They are mostly used in digital computers, radars and television.
- They are of 4 types.
  - Positive clipper
  - Negative Clipper
  - Biased Clipper
  - Combination Clipper.

Positive clippers:

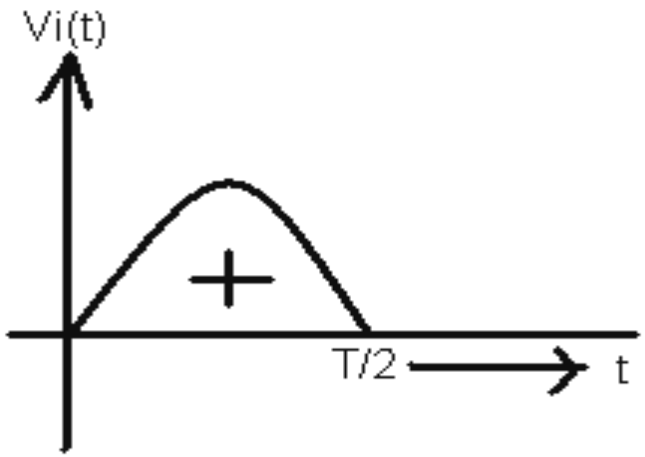


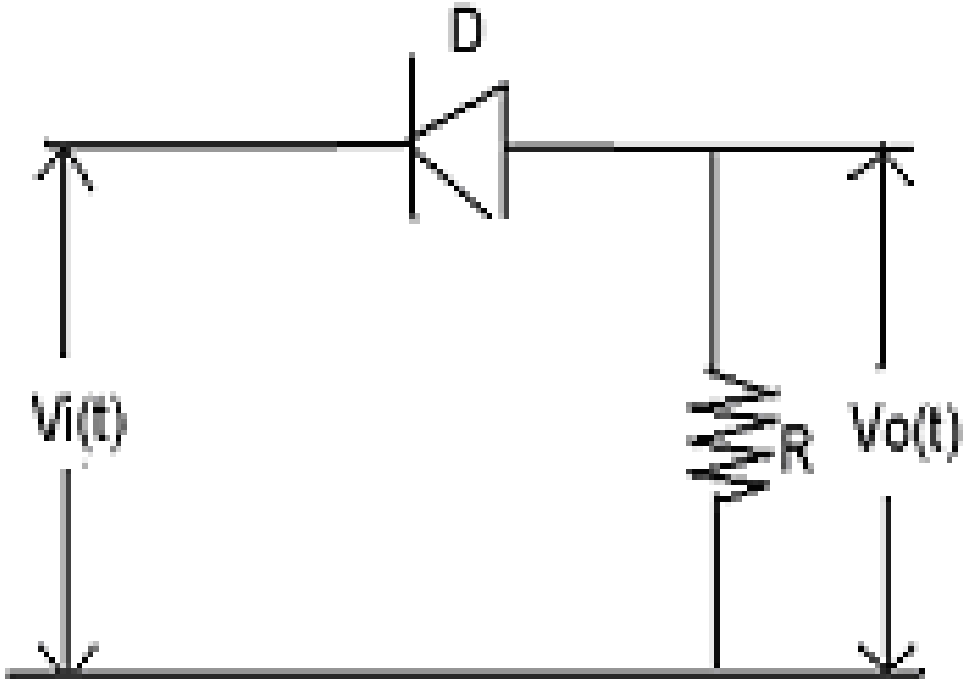


Analysis

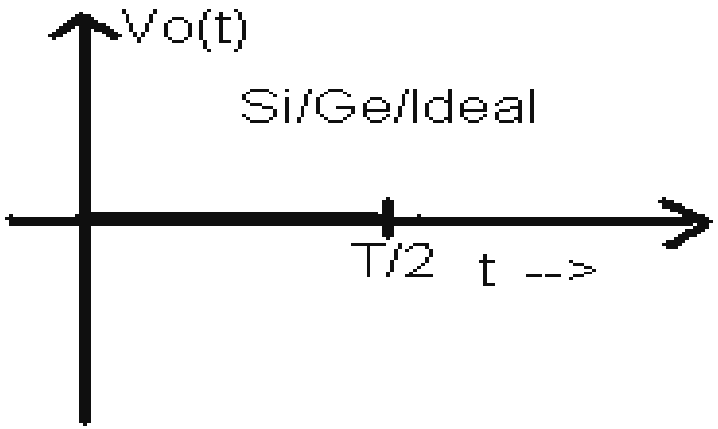
For the analysis of the clipper circuits, each half cycles of the input signal must be considered individually.

FOR +Ve HALF CYCLE

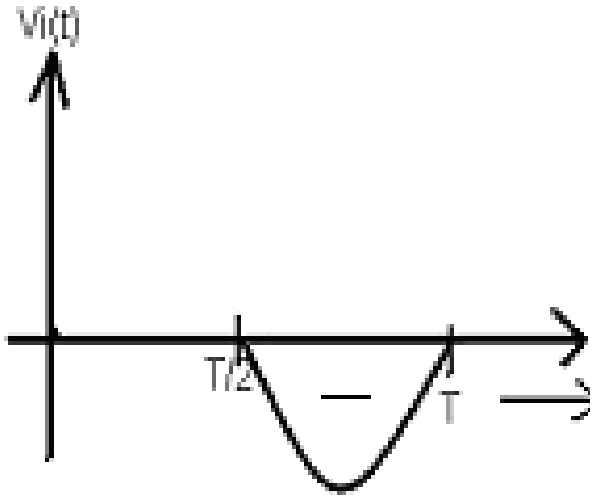


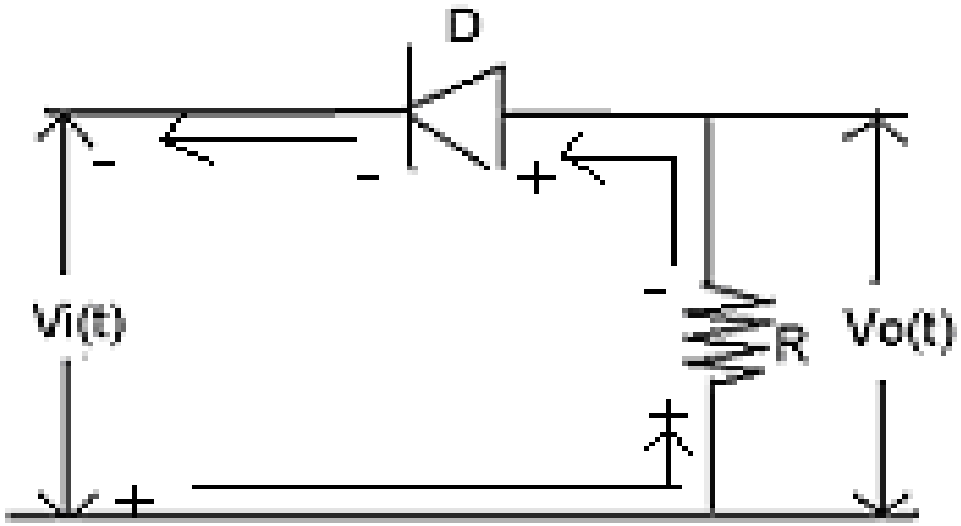


- For the +Ve Half cycle of input signal, the general Diodes are reverse biased and hence no current flow
- Therefore, $I_d = 0v$ and $V_R = I_d \times R = 0v$, i.e. no output waveform for +Ve half cycle



FOR -Ve HALF CYCLE





- For the -Ve Half cycle of input signal, the diode is forward biased.

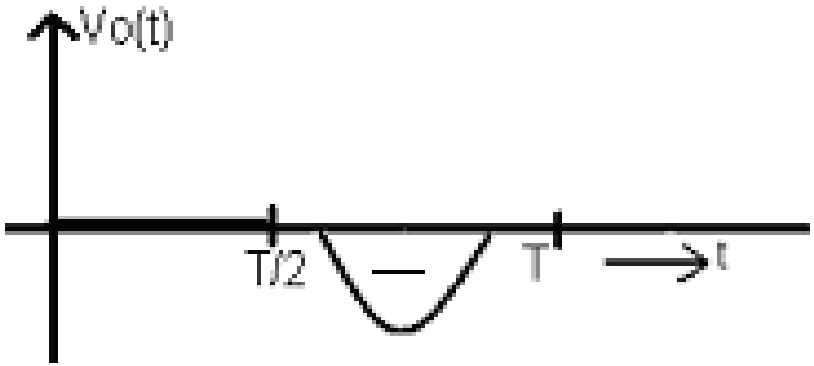
- By applying KVL in the loop, we get

$$V_i(t) - V_o - V_D = 0$$

$$\Rightarrow V_0 = V_i(t) - V_D$$

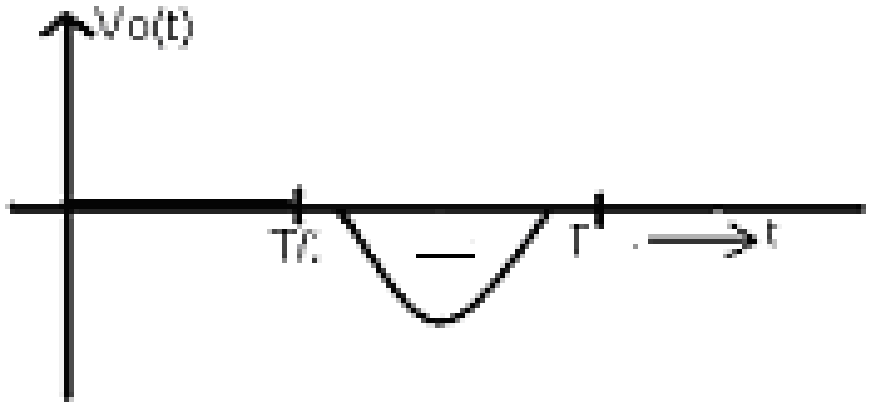
If the diode is assumed, Si; Then the output voltage wave form will be

$$V_0 = V_i(t) - 0.7v$$



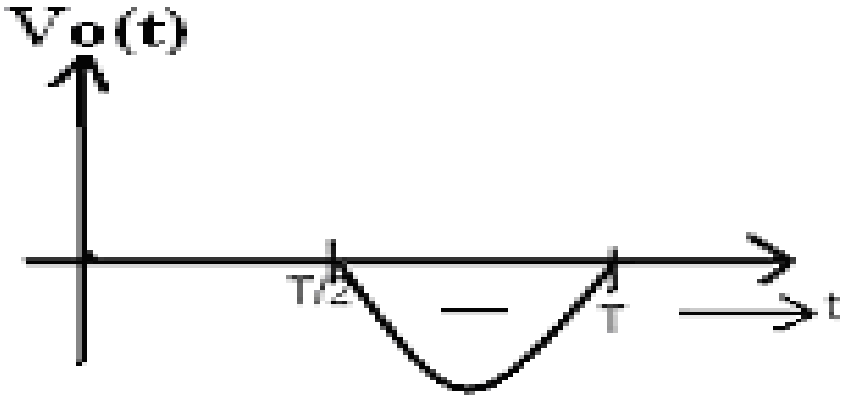
If the diode is assumed, Ge; Then the output voltage wave form will be

$$V_0 = V_i(t) - 0.3v$$

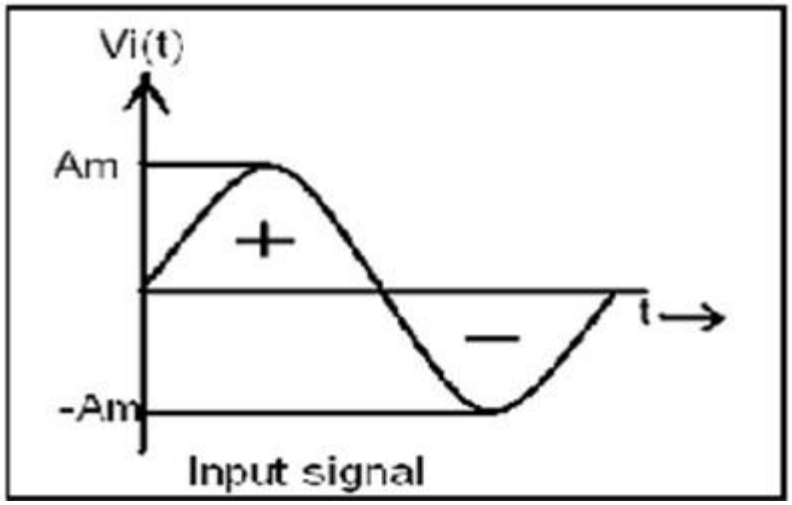


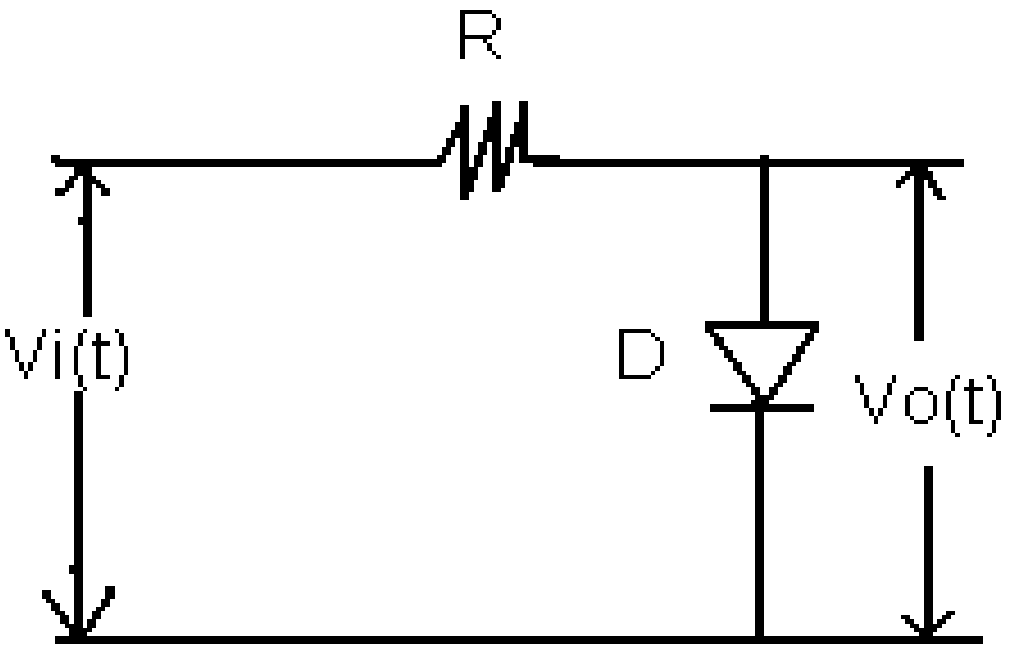
If the diode is assumed, Ideal; Then the output voltage wave form will be

$$V_0 = V_i(t) - 0\ v = V_i(t)$$

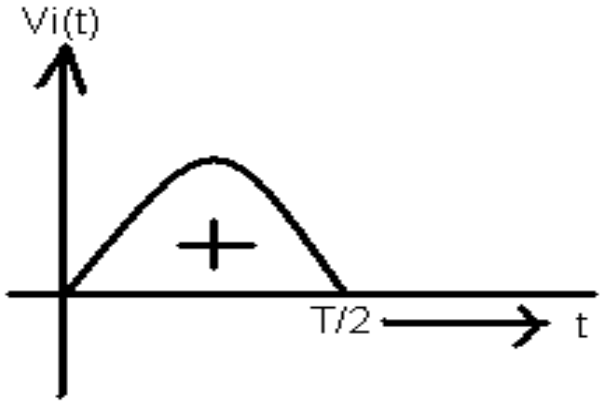


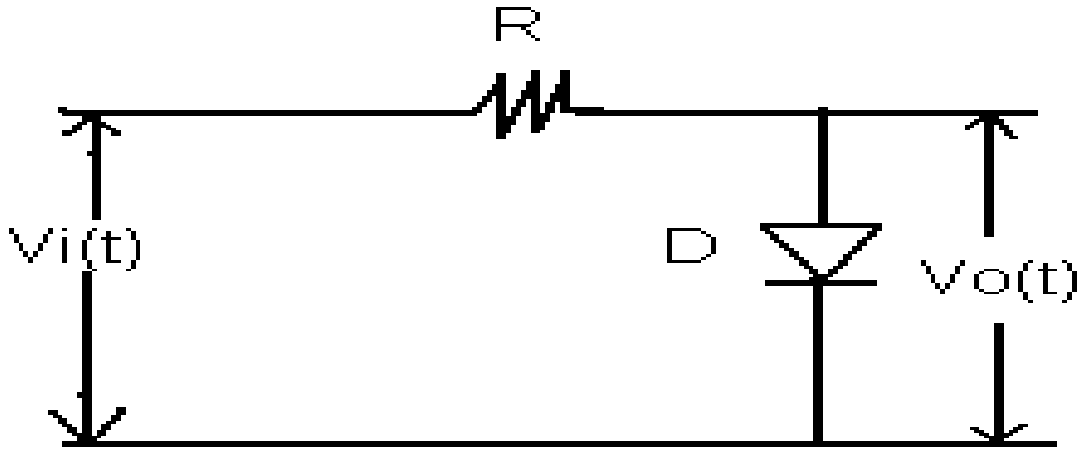
Positive clippers:





FOR +Ve HALF CYCLE



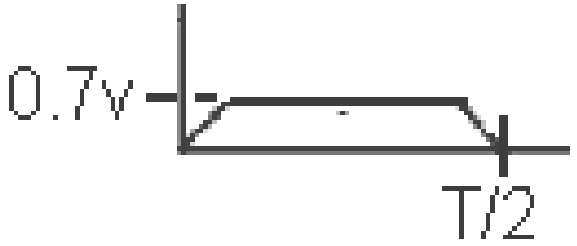


For the +Ve Half cycle of input signal, the general Diodes are Forward biased and hence current will flow.

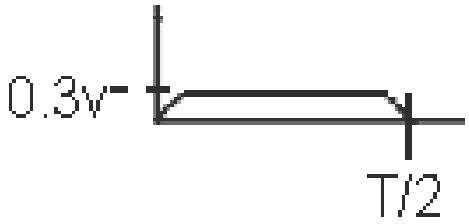
Since the Diode is Forward Biased, The Depletion voltage will drop across the Diode e.g. for Si diode (0.7v), for Ge Diode (0.3v), for Ideal diode (0v).

From the circuit, again the output voltage (V_o (t)) is same as the diode voltage.

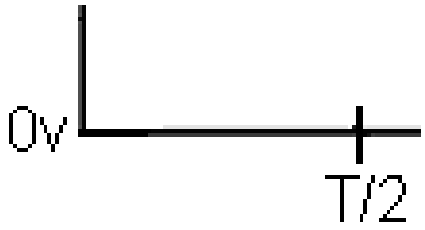
If the diode is assumed, Si; Then the output voltage wave form will be



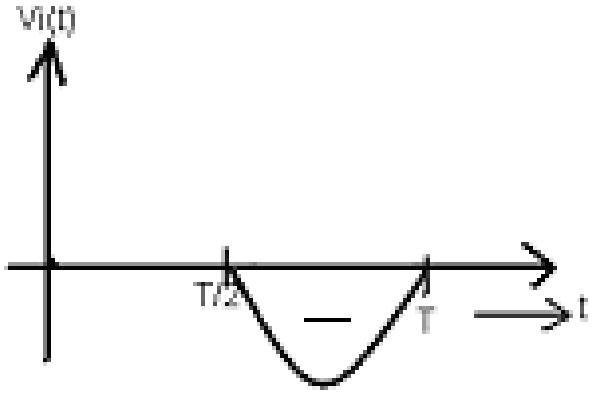
If the diode is assumed, Ge; Then the output voltage wave form will be

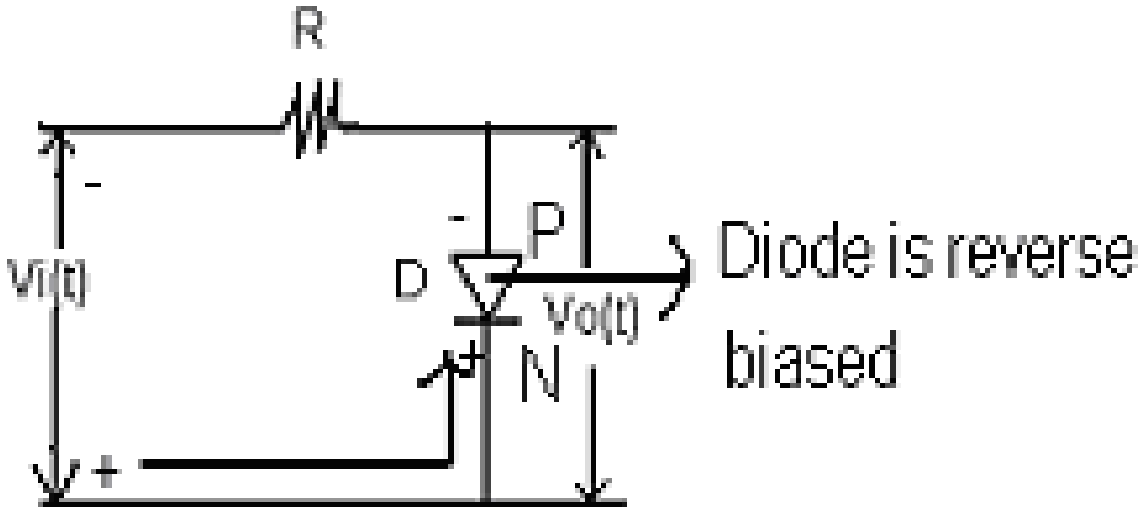


If the diode is assumed, Ideal; Then the output voltage wave form will be



FOR –Ve HALF CYCLE

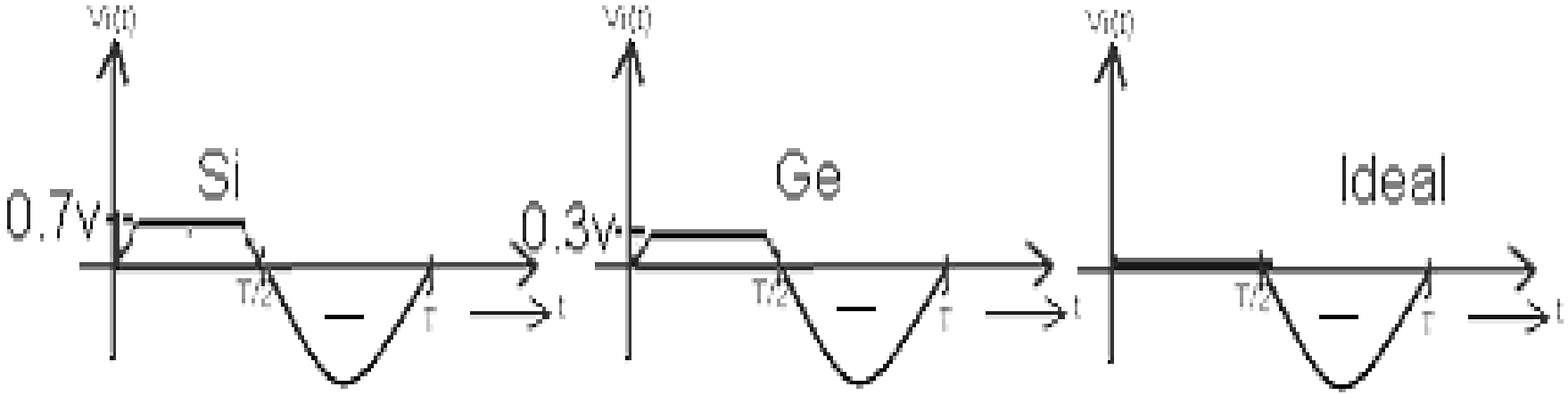




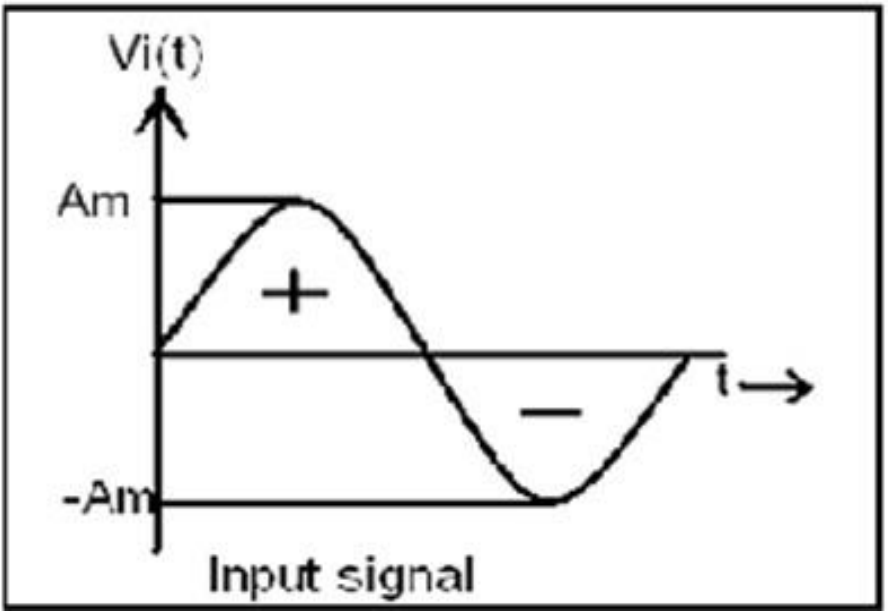
For the -Ve Half cycle of input signal, the diode is reverse biased.

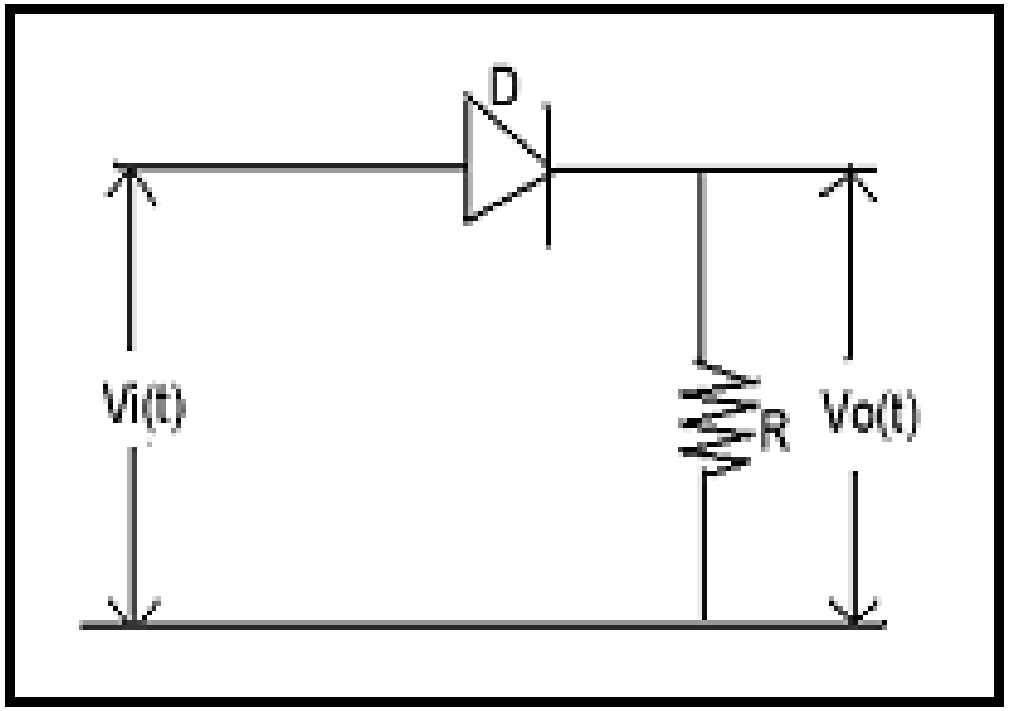
Therefore, $I_d = 0v$ and $V_R = I_d \times R = 0v$

The net outputs for the input signal Vi(t)[for different Diodes] are



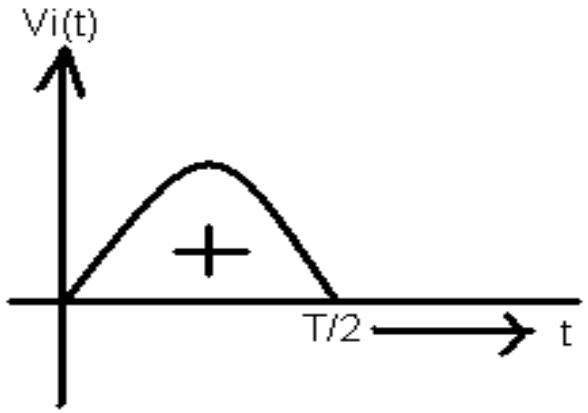
Negative clippers:

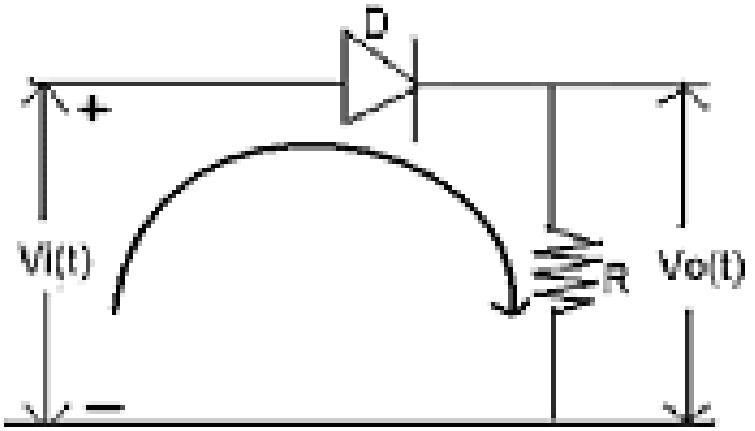




Analysis

FOR +Ve HALF CYCLE





KVL

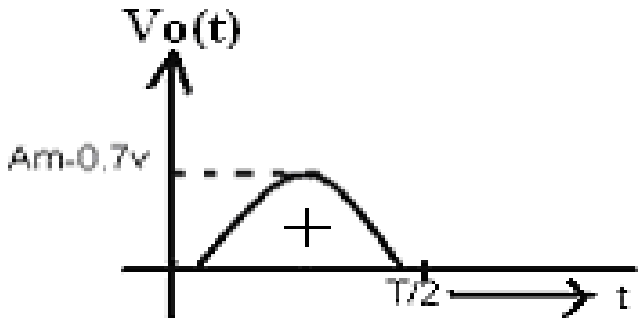
$Vi(t) - V_D - V_R = 0$

$\Rightarrow V_R = Vi(t) - V_D$

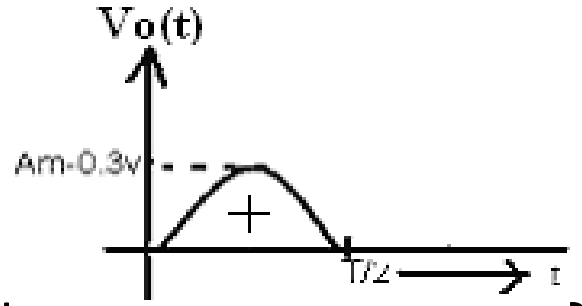
Since, $V_o(t) = V_R$

Therefore, $Vo(t) = V_i(t) - V_D$

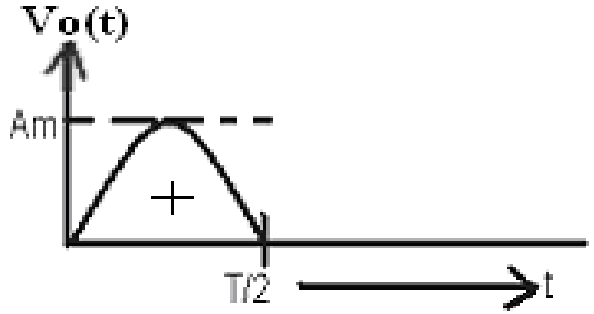
If the diode is assumed, Si; Then the output voltage wave form will be



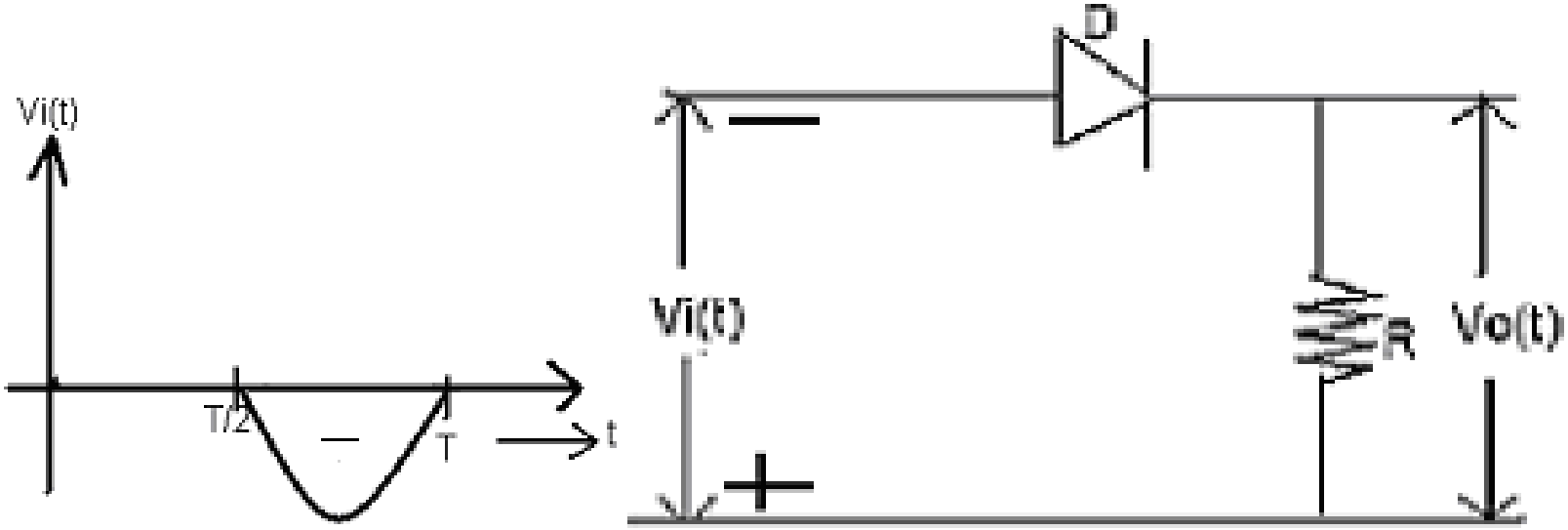
If the diode is assumed, Ge; Then the output voltage wave form will be



If the diode is assumed, ideal; then the output voltage wave form will be

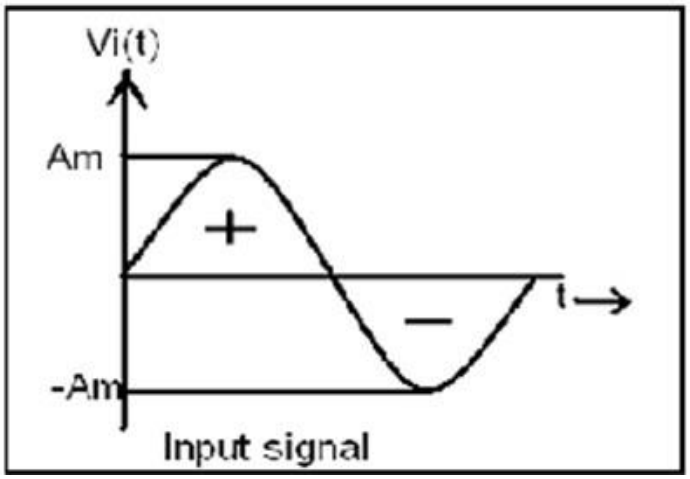


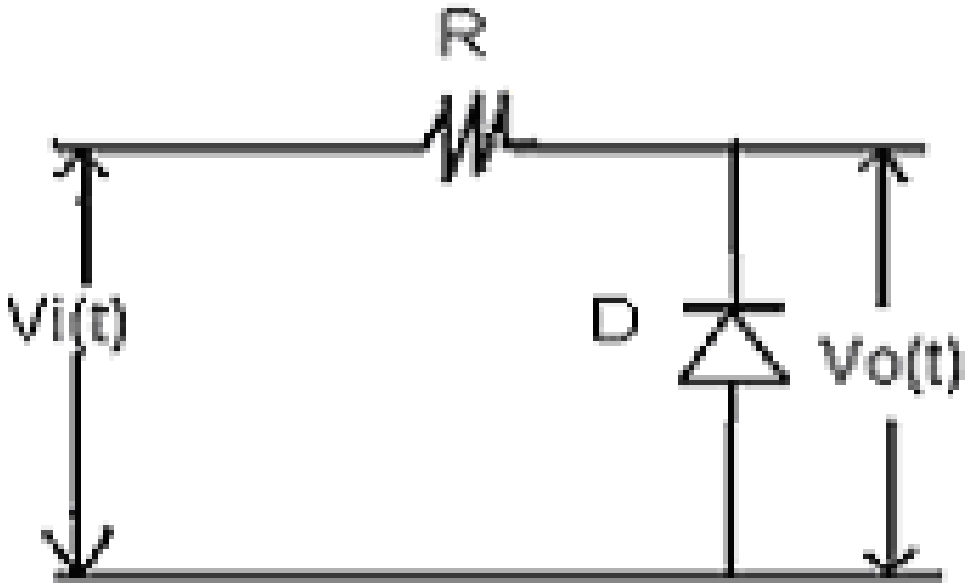
FOR –Ve HALF CYCLE



- In –Ve half cycle the Diode is reverse Biased and hence no current flow in the path.
- Therefore, Id=0mA And $V_R = V_o(t) = 0v$

Negative clippers:



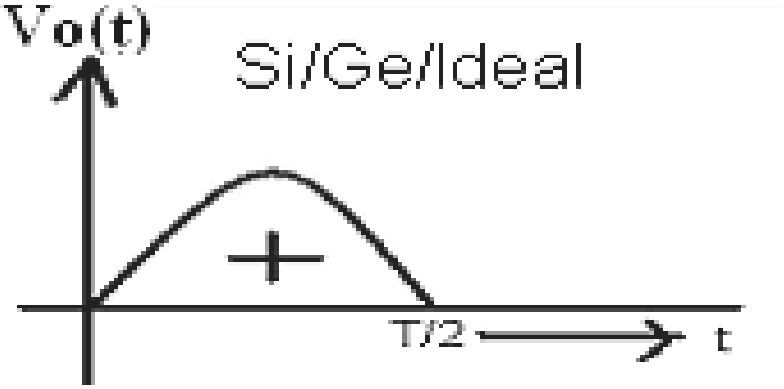


Analysis

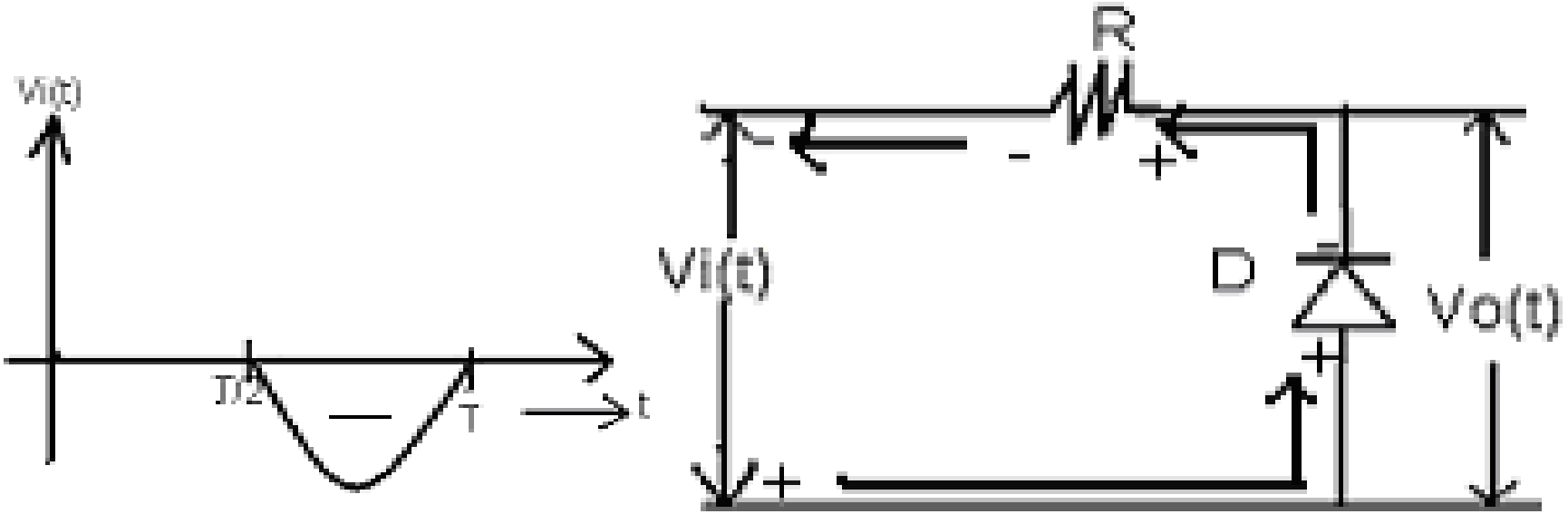
FOR +Ve HALF CYCLE

For the +Ve Half cycle of input signal, the general Diodes are reverse biased and hence no current flow. Therefore, $I_d = 0v$ and $V_R = I_d \times R = 0v$

$Vo(t) = V_D$ = Maximum voltage drop due to open ckt



FOR –Ve HALF CYCLE



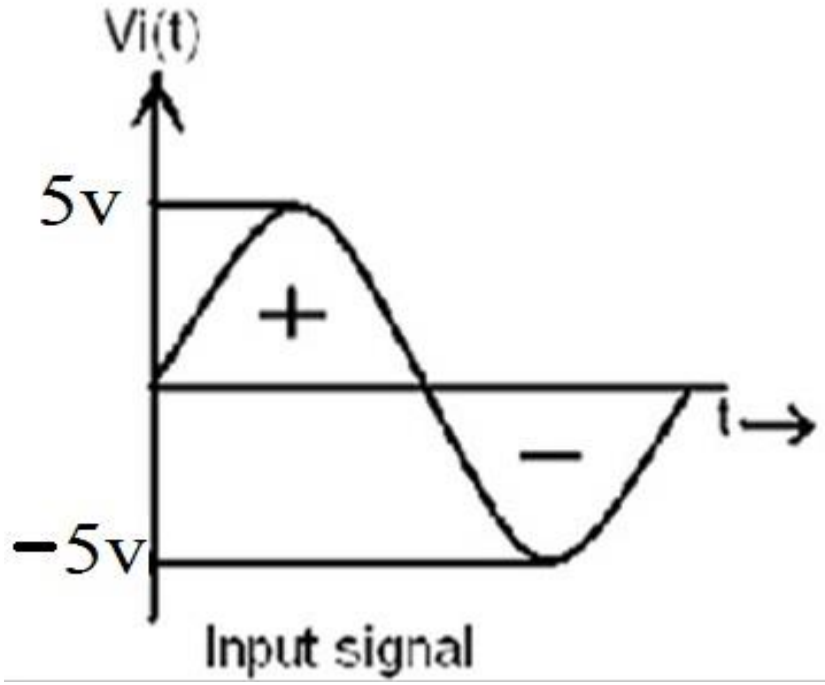
For the –Ve Half cycle of input signal, the diodes is Forward biased and hence current will flow.

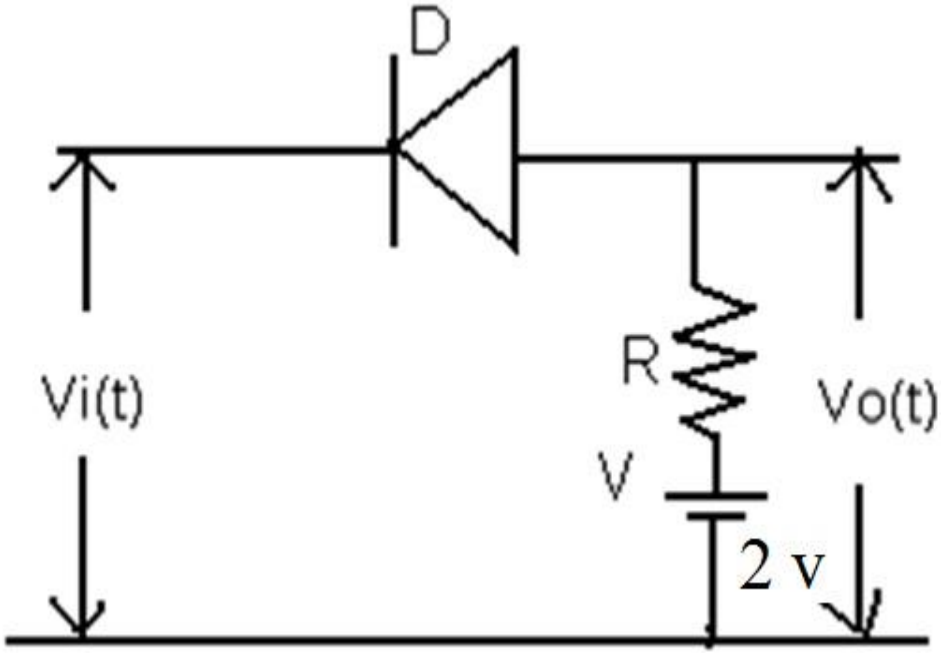
Since the Diode is Forward Biased, The Depletion voltage will drop across the Diode e.g. for Si diode (0.7v), for Ge Diode (0.3v) ,for Ideal diode (0v).

Here the output voltage ($V_o(t)$) is same as the diode voltage

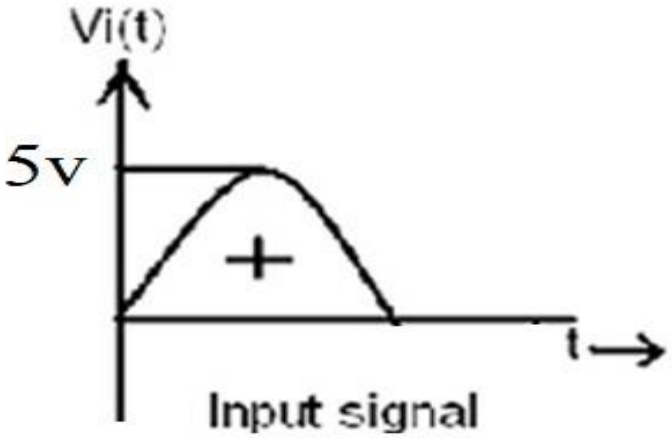
1.Biased clippers:

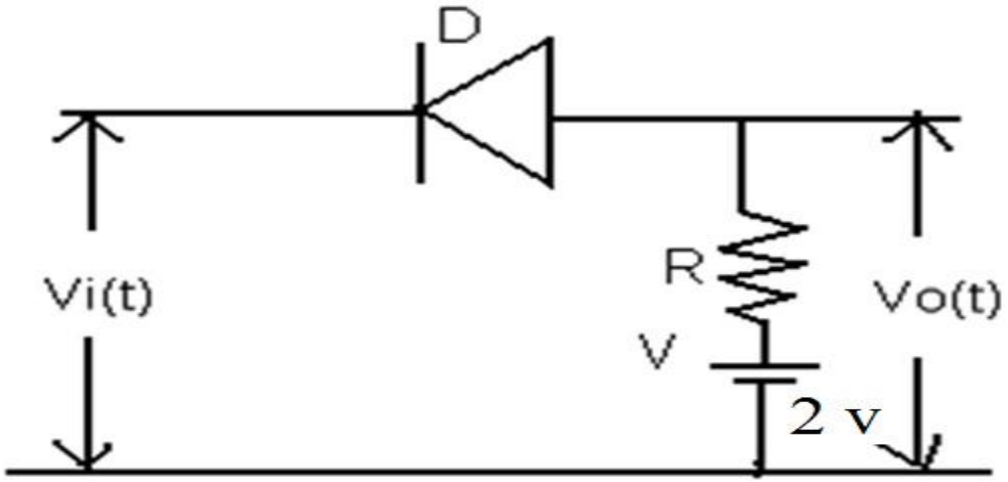
Draw the output waveform for the given circuit assuming the diode as Si type, Ge type & Ideal.





FOR +Ve HALF CYCLE





As we know that the input signal is higher than the biased voltage. Therefore,

For the +Ve half cycle, the diode is reverse biased and hence no current flow in the path of resistor.

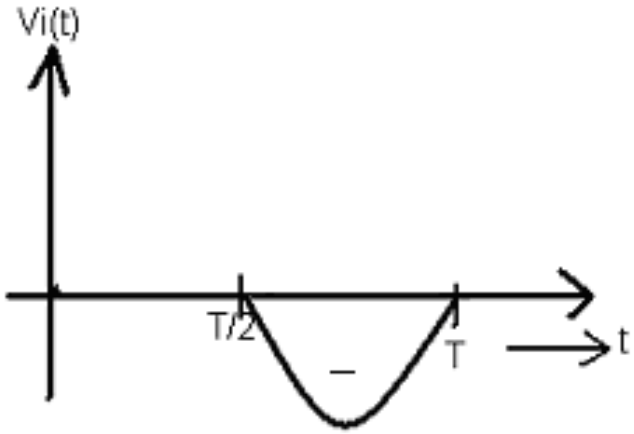
$I_d = 0v$

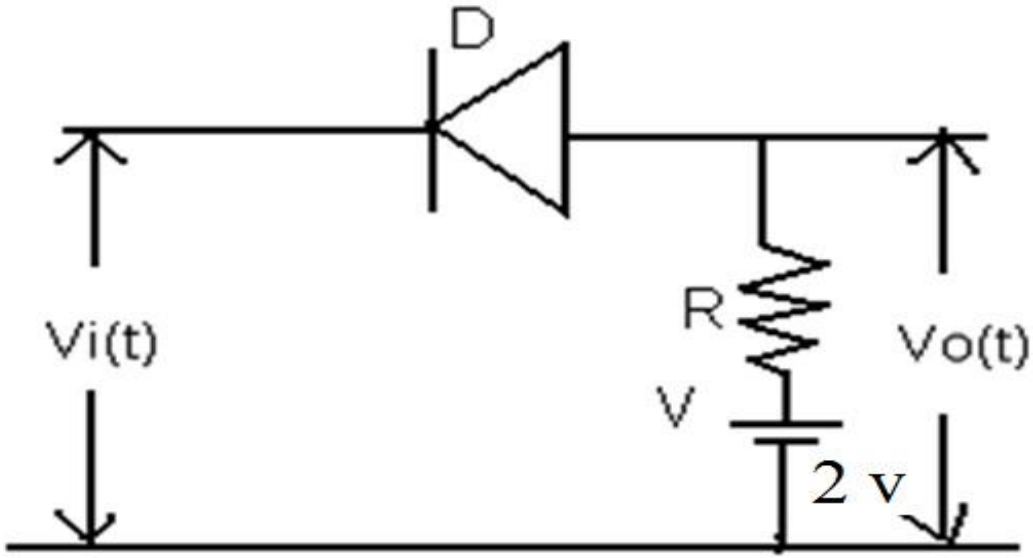
$V_R = I_d \times R = 0 \times R = 0v$

Since, $V_o(t) = V_R + 2V$ (because of parallel open loop voltage)

Therefore, $V_o(t) = V_R + V = 0v + 2V = 2\ V$

FOR –Ve HALF CYCLE





In –Ve Half cycle the Diode is Forward Biased and hence, there will be a current flow in the path.

Therefore, according to KVL, we get

$$V_i(t) + V - V_R - V_D = 0$$

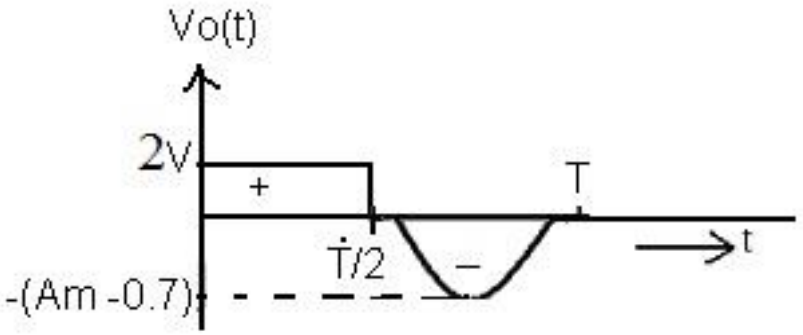
$$=> V_R = V_i(t) + V - V_D$$

Now, we have

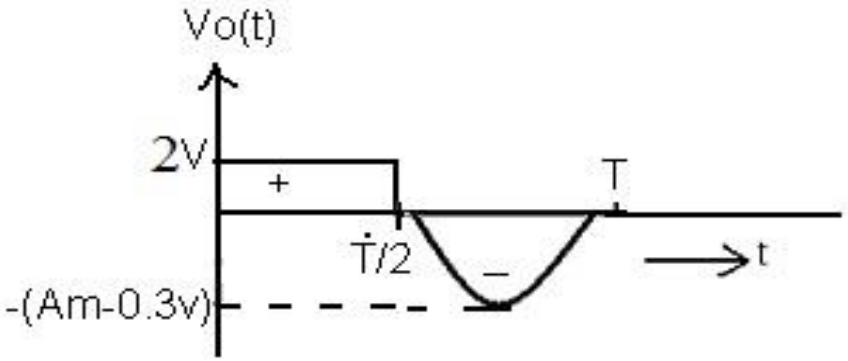
$$V_o(t) = V_R - V$$

There fore, $V_o(t) = V_R - V = V_i(t) - V_D + V - V = V_i(t) - V_D$

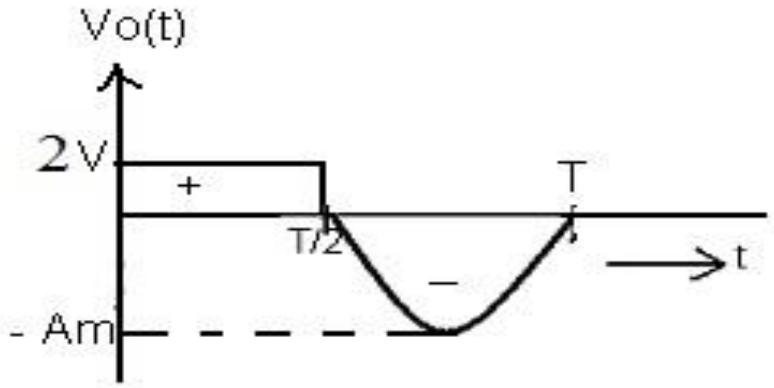
If the diode is Si;



If the diode is Ge;

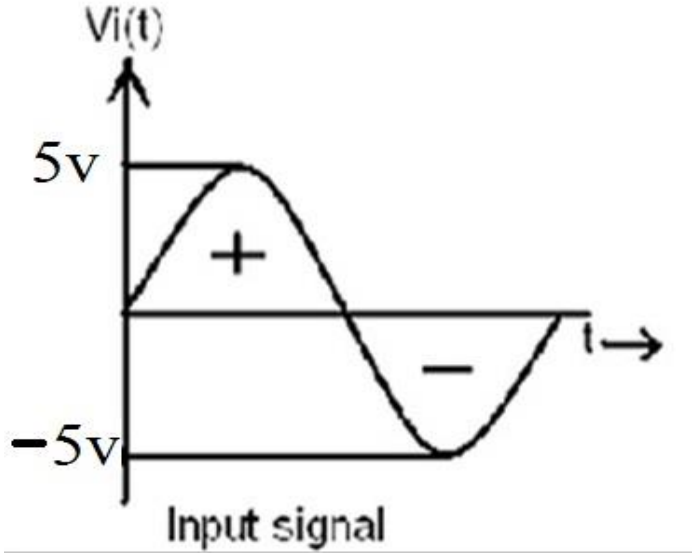


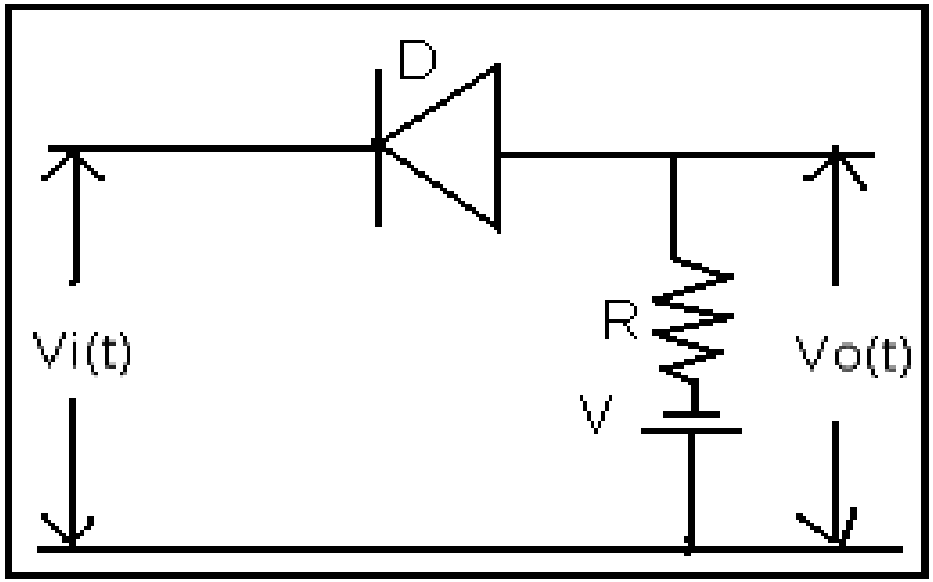
If the diode is Ideal;



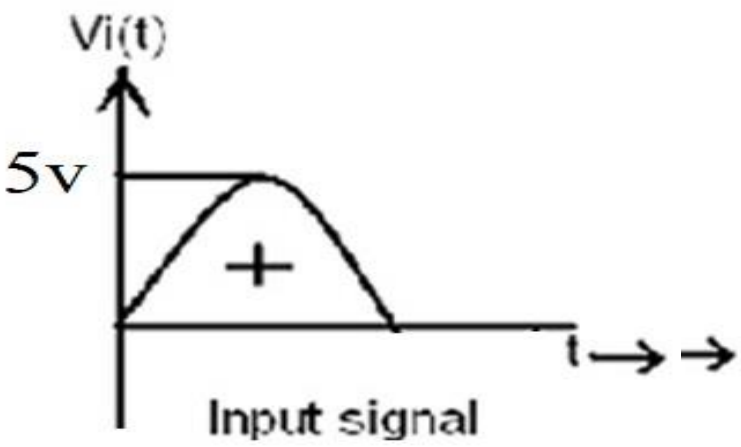
2.Biased clippers:

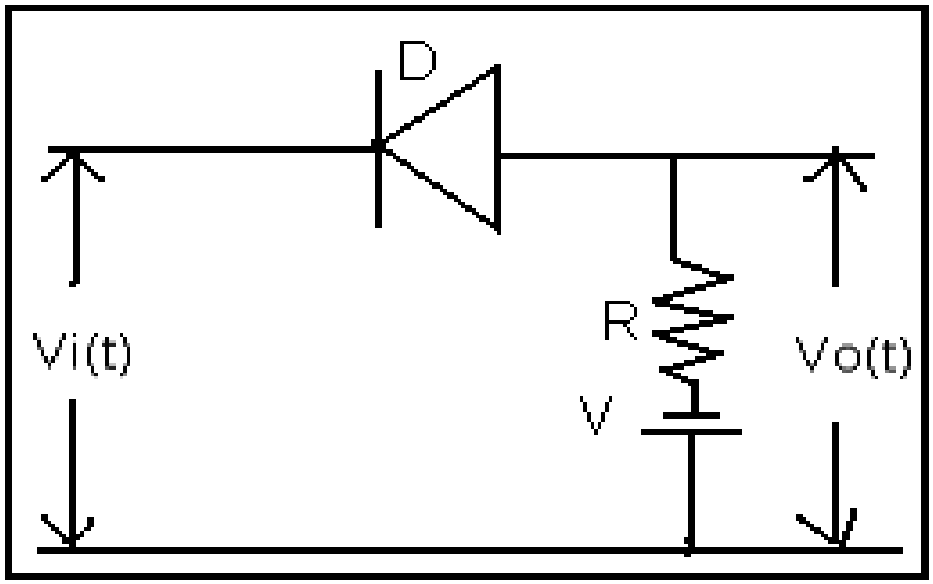
Draw the output waveform for the given circuit assuming the diode as Si type, Ge type & Ideal.





FOR +Ve HALF CYCLE



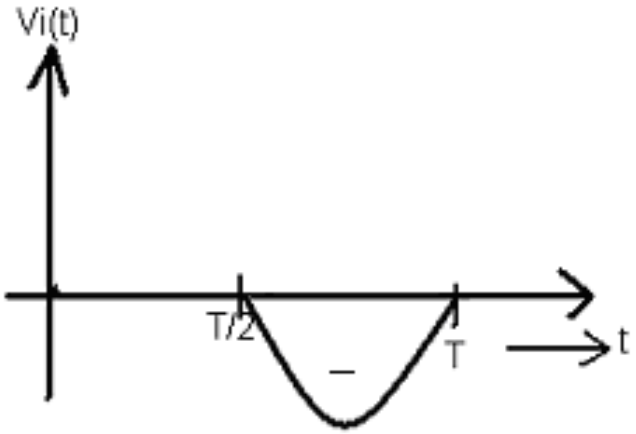


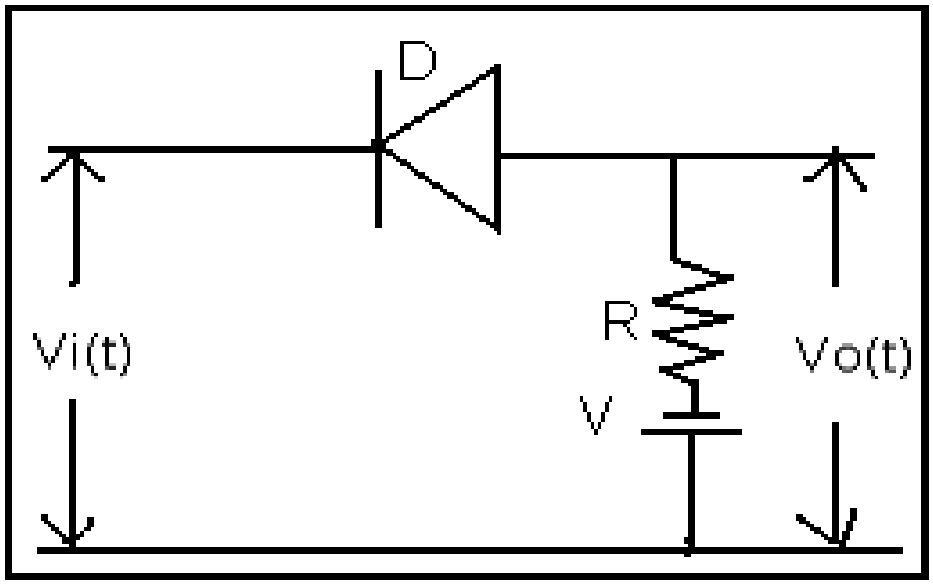
Diode is reverse biased

$\Rightarrow$ I = 0 => IR = 0 => No voltage drop across the resistor

$\Rightarrow$ Vo = - V

FOR –Ve HALF CYCLE





Diode is forward biased.

By KVL,

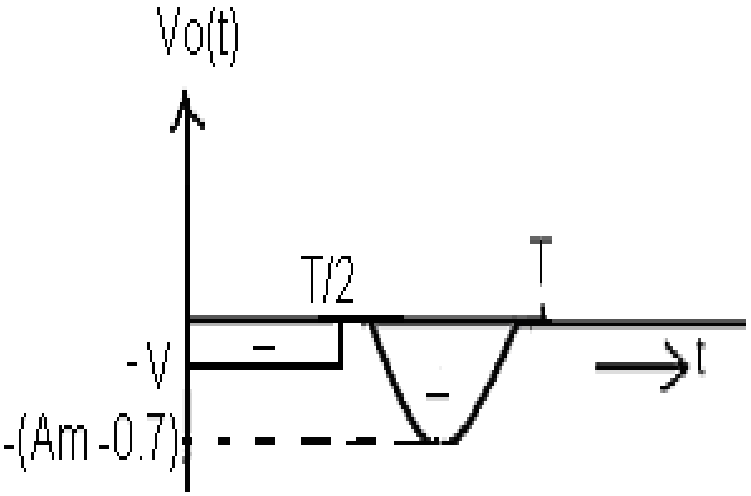
$Vi - V - IR - V_D = 0$

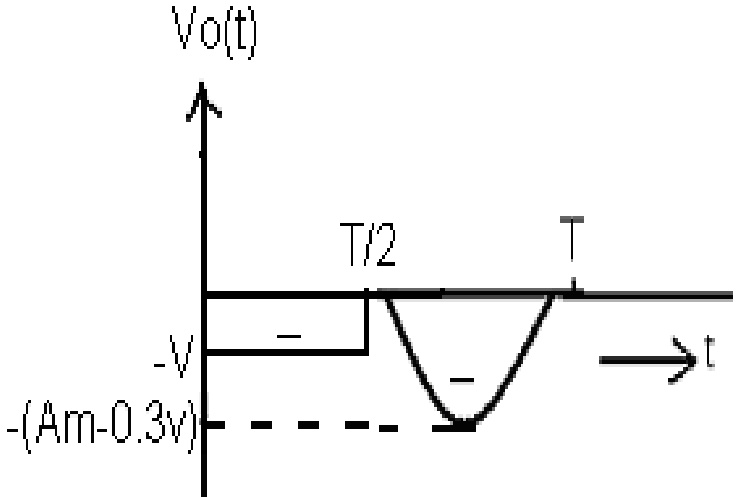
$\Rightarrow Vi - V_D - (V+IR) = 0$

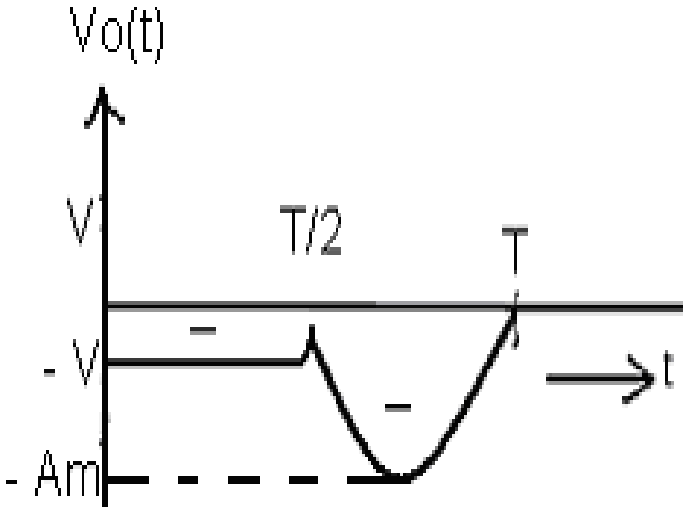
$\Rightarrow Vi - V_D - Vo = 0$

$\Rightarrow Vo = Vi - V_D$

If the diodes are assumed, Si, Ge, Ideal; Then the output voltage wave forms are

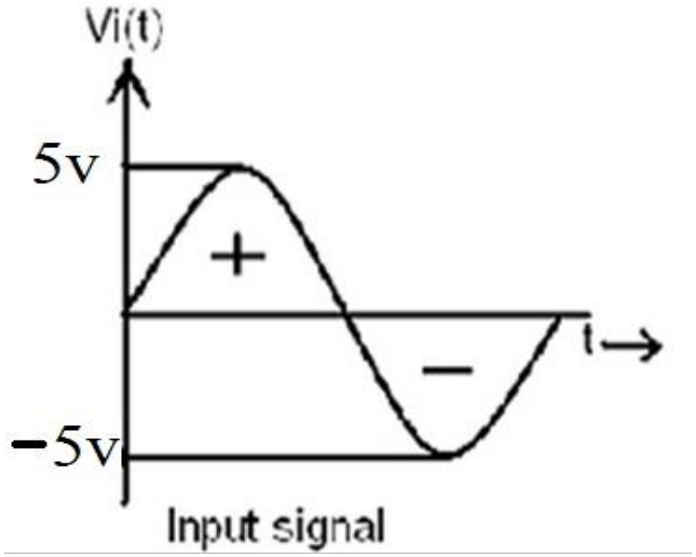


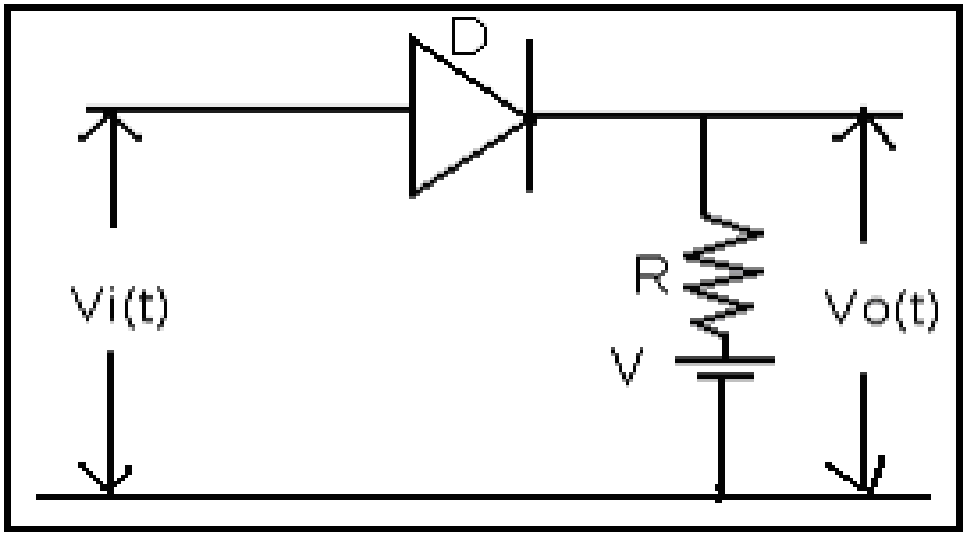




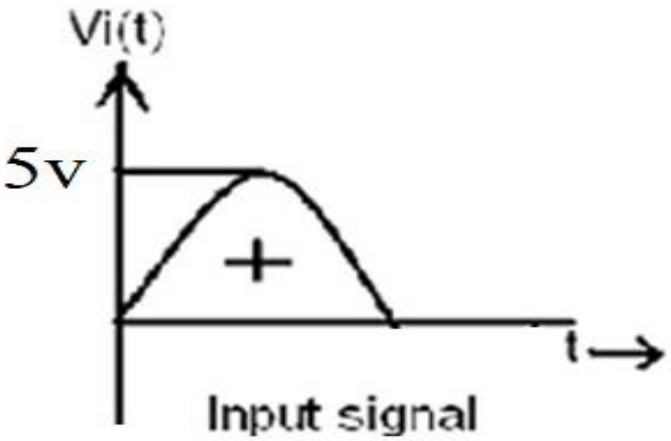
3.Biased clippers:

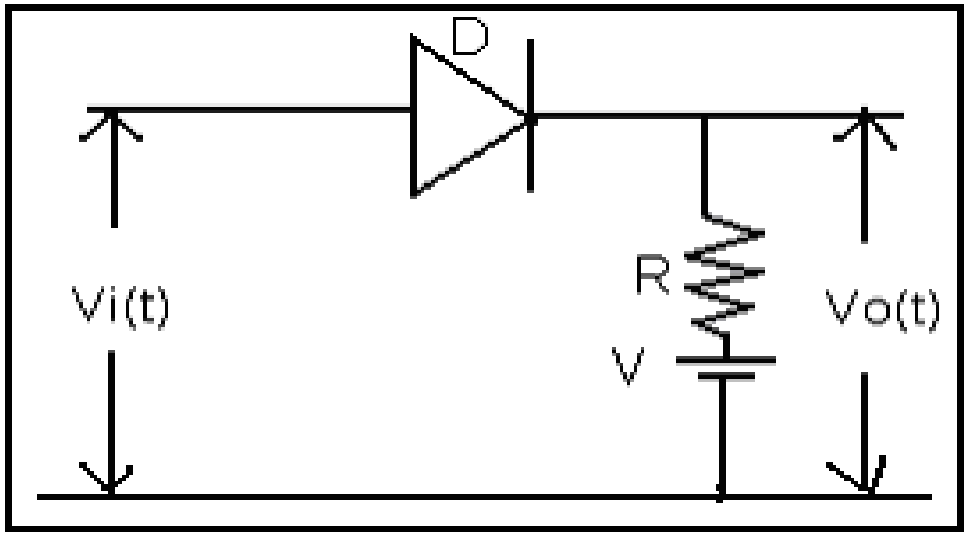
Draw the output waveform for the given circuit assuming the diode as Si type, Ge type & Ideal.





FOR +Ve HALF CYCLE





Diode is forward biased.

By KVL,

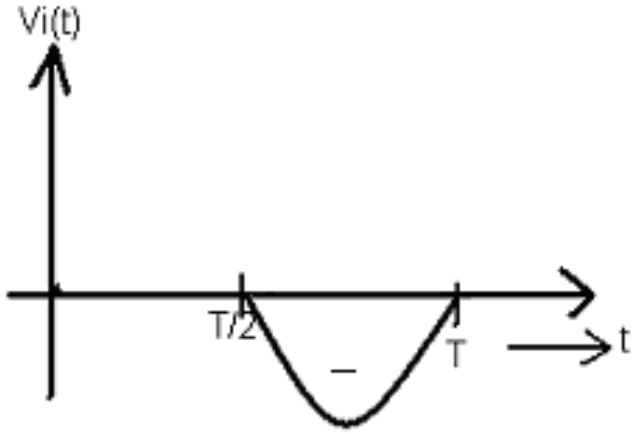
$Vi - V_D - IR - V = 0$

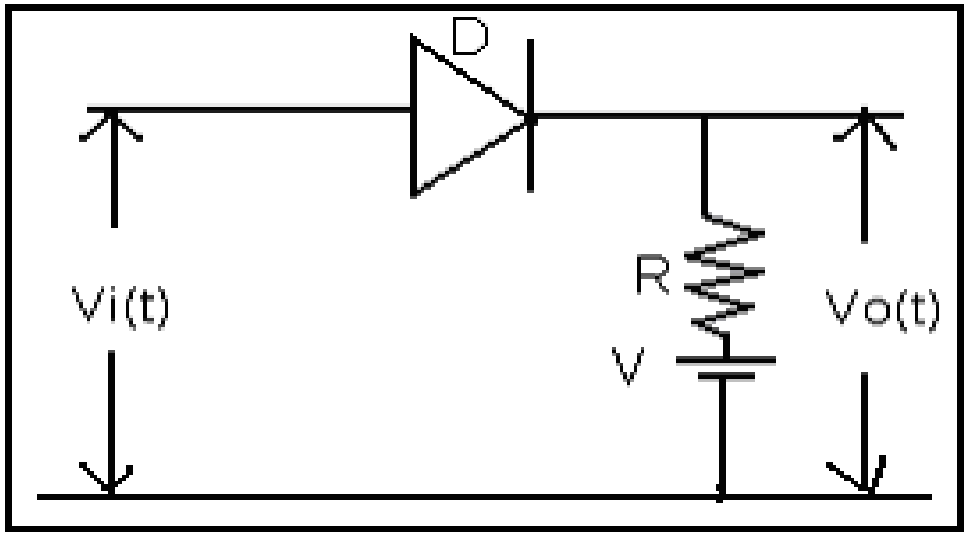
$\Rightarrow Vi - V_D - (IR + V) = 0$

$\Rightarrow Vi - V_D - Vo = 0$

$\Rightarrow Vo = Vi - V_D$

FOR -Ve HALF CYCLE





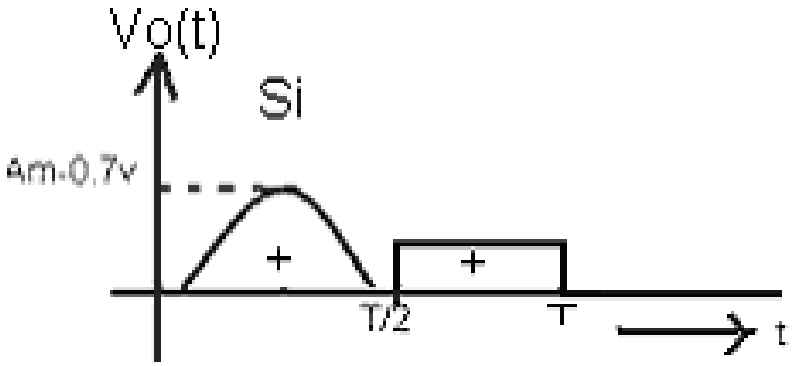
Diode is reverse biased.

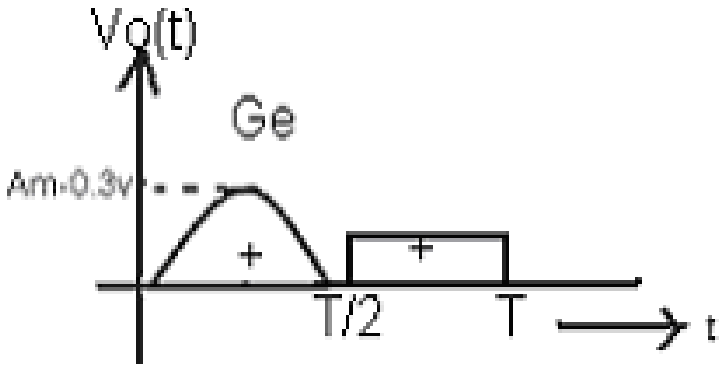
$\Rightarrow$ I = 0

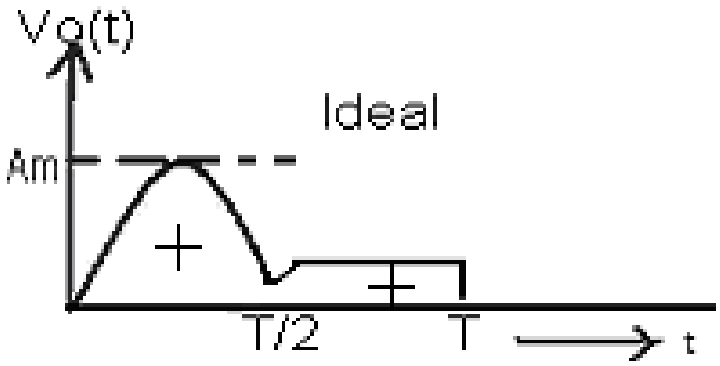
$\Rightarrow$ IR = 0 => No voltage drop across the resistor.

$\Rightarrow$ Vo = V

The net output for the given input signal

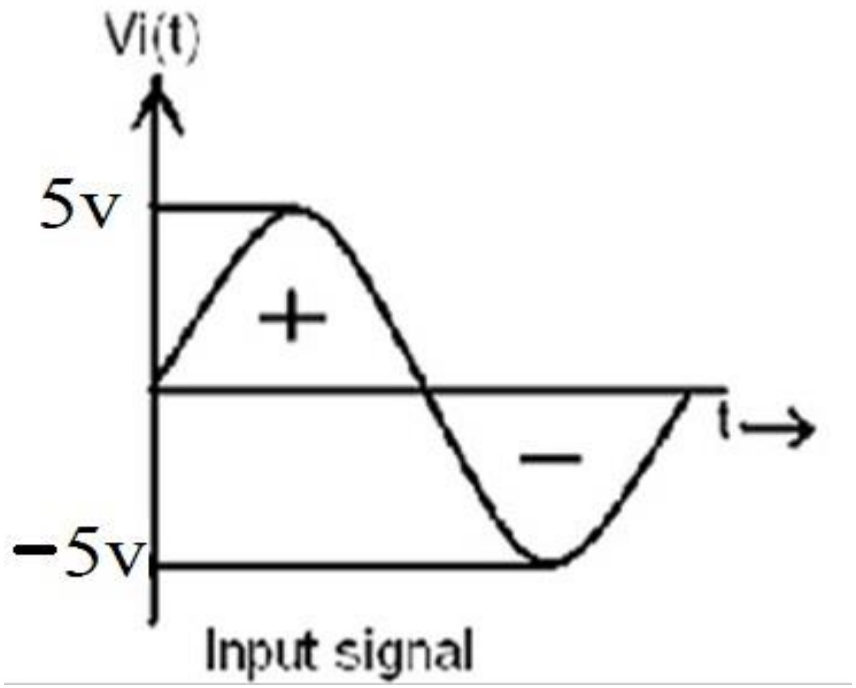


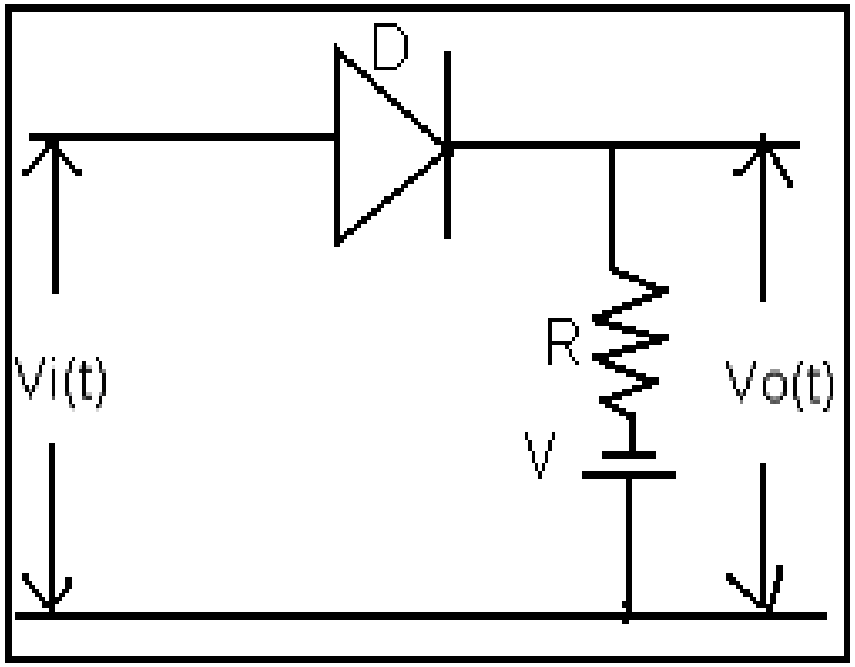




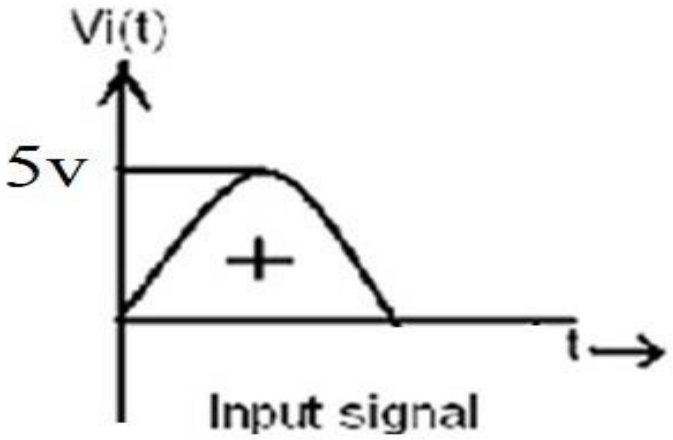
4.Biased clippers:

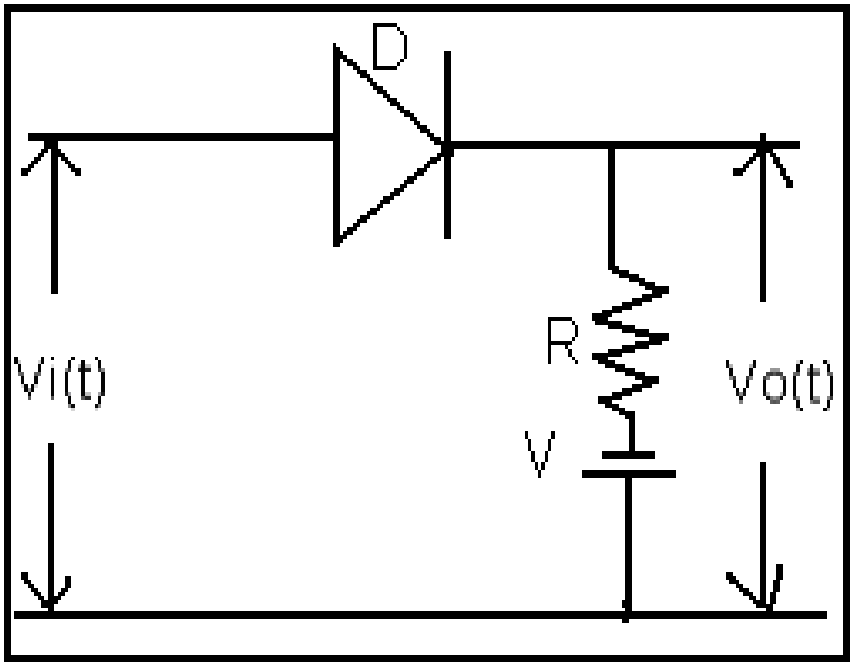
Draw the output waveform for the given circuit assuming the diode as Si type, Ge type & Ideal.





FOR +Ve HALF CYCLE





By KVL

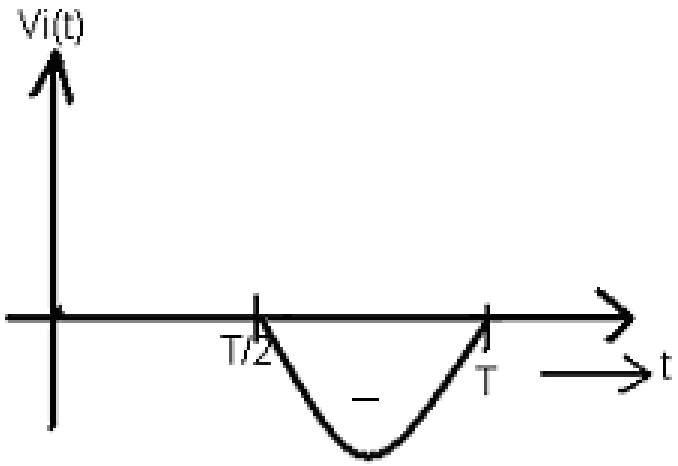
$Vi(t) - V_D - V_R + V = 0$

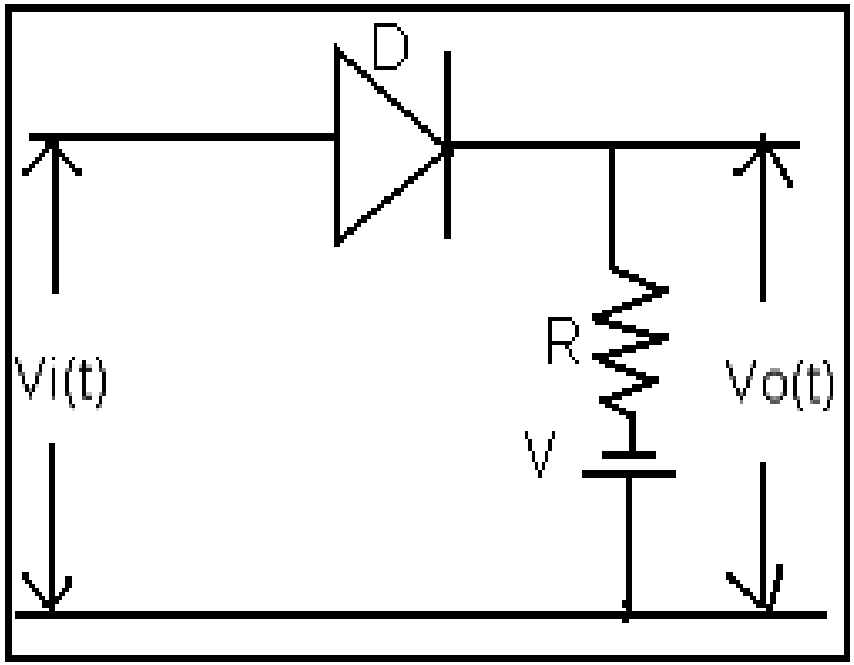
$\Rightarrow Vi(t) - V_D - (V_R - V) = 0$

$\Rightarrow Vi(t) - V_D - V_o(t) = 0$

$\Rightarrow V_o(t) = Vi(t) - V_D$

FOR –Ve HALF CYCLE



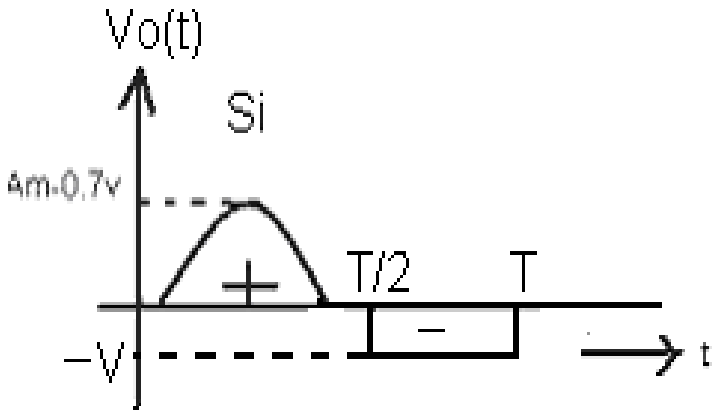


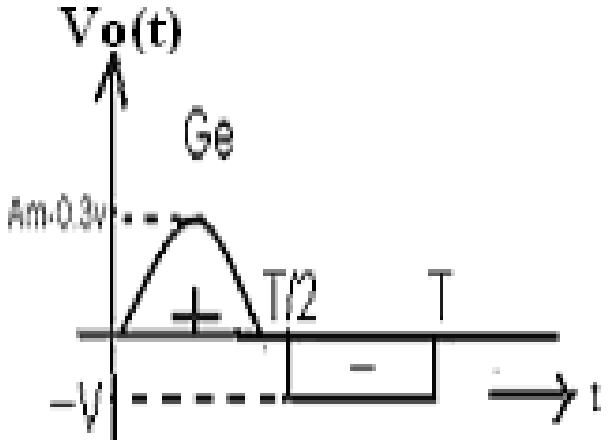
Diode is reverse biased.

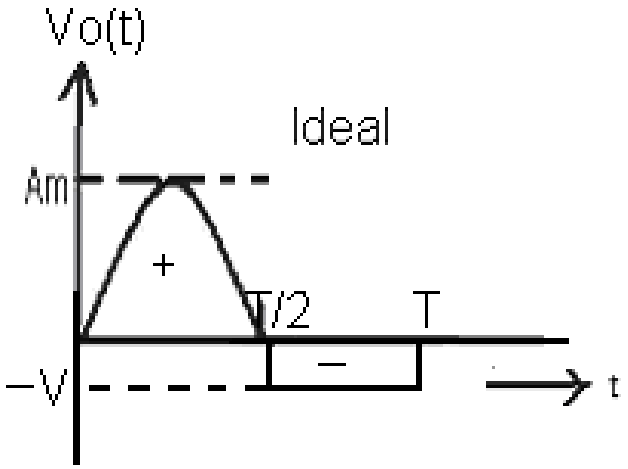
$\Rightarrow$ No current in the loop => $V_R = 0$

$\Rightarrow V_o(t) = - V$

The net output for the given input signal

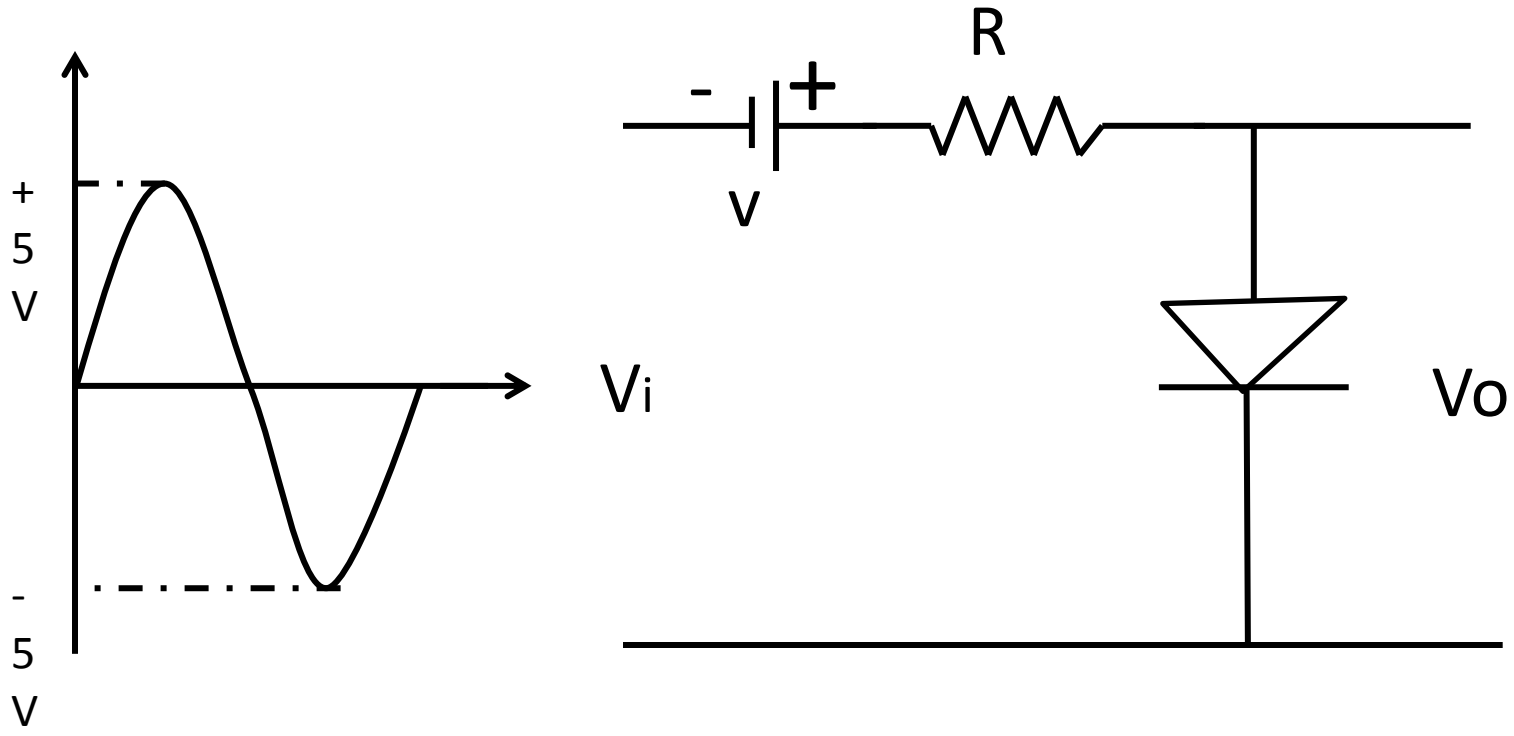




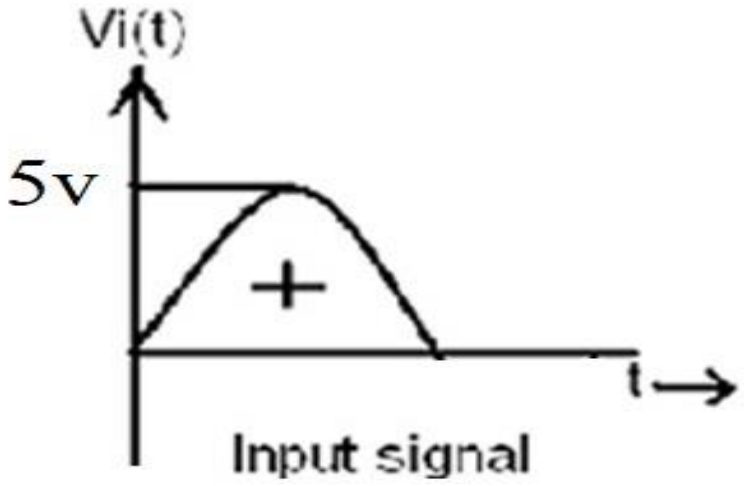


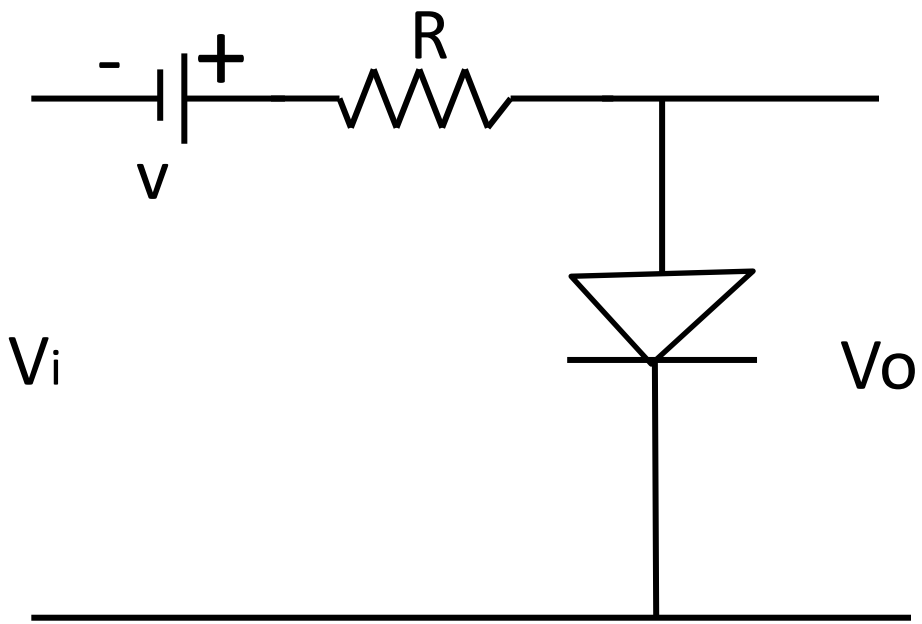
5. Biased clippers:

Draw the output waveform for the given circuit assuming the diode as Si type, Ge type & Ideal.



For +ve half cycle

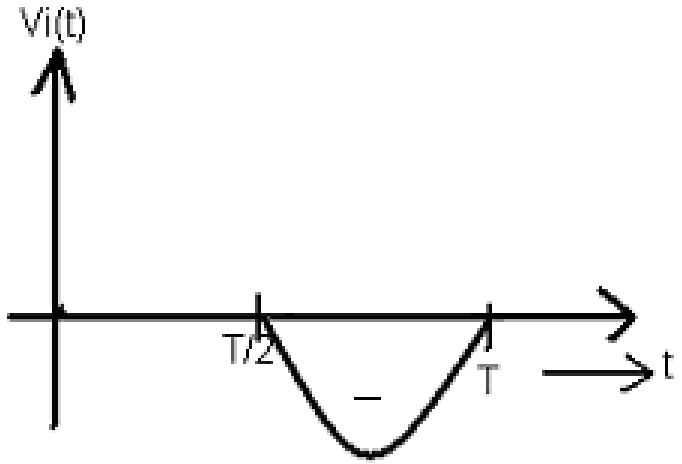


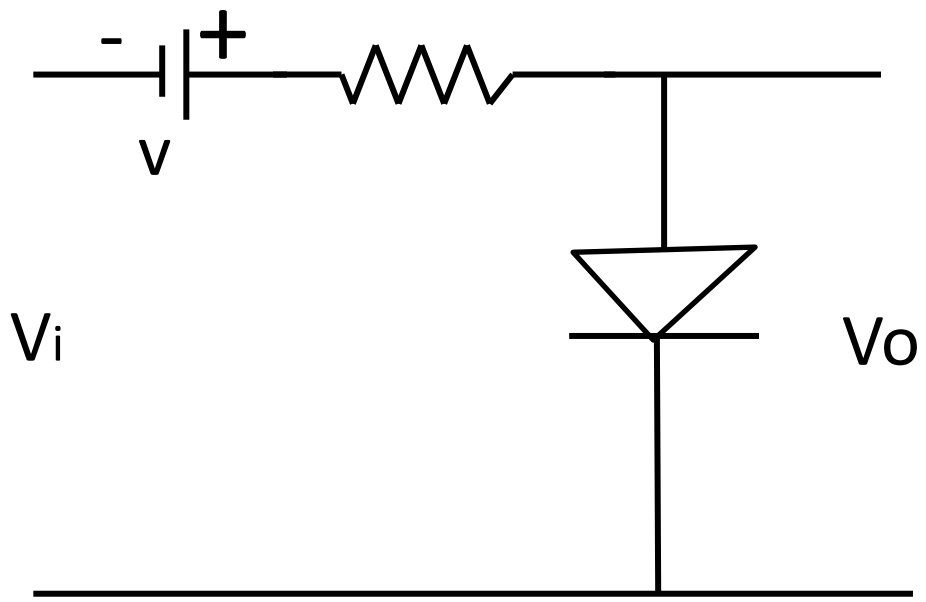


Diode is forward biased.

Here $V_0 = V_D = 0.7$ for Si / 0.3 for Ge / 0 when diode is ideal

For -ve half cycle





Diode is Reverse biased.

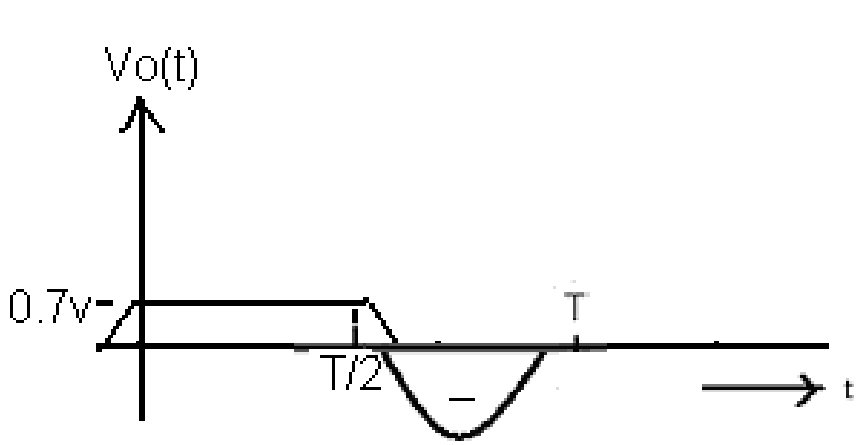
Hence I = 0 => $V_R = 0$.

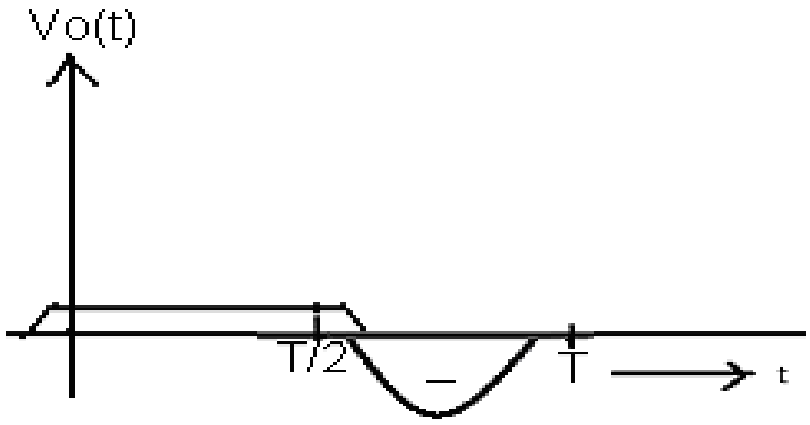
So by KVL

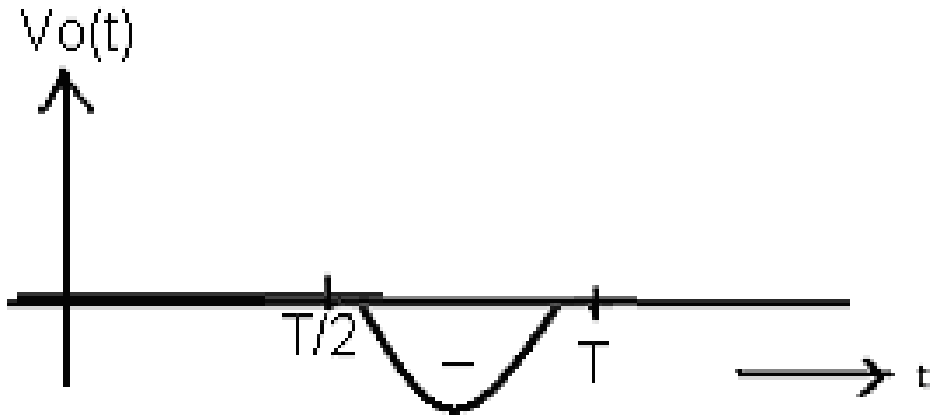
– Vi(t) + V – Vo(t) = 0

=> Vo(t) = V – Vi(t)

The net output for the given input signal

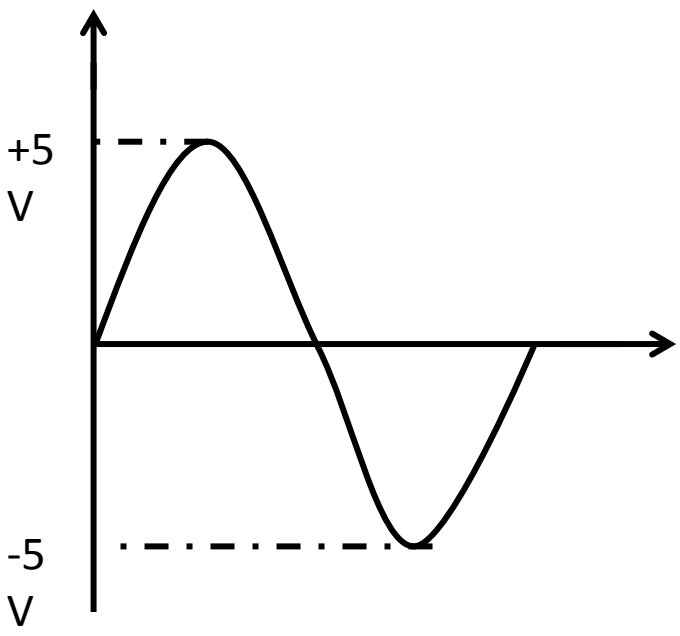


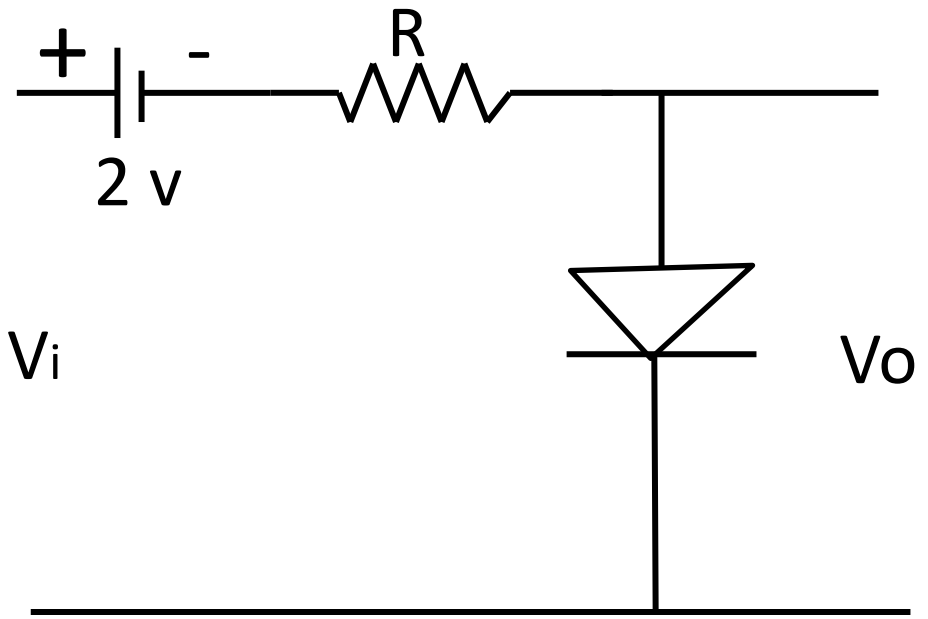




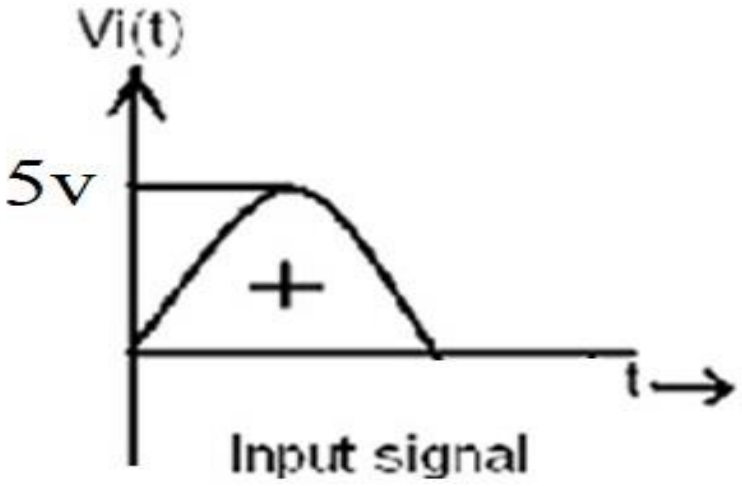
6. Biased clippers:

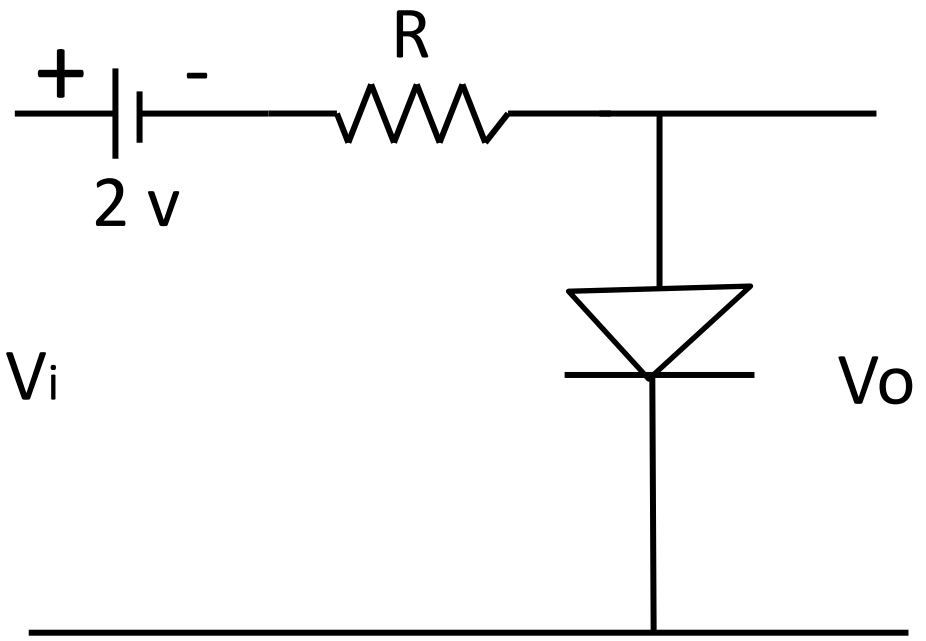
Draw the output waveform for the given circuit assuming the diode as Si type, Ge type & Ideal.





For +ve half cycle

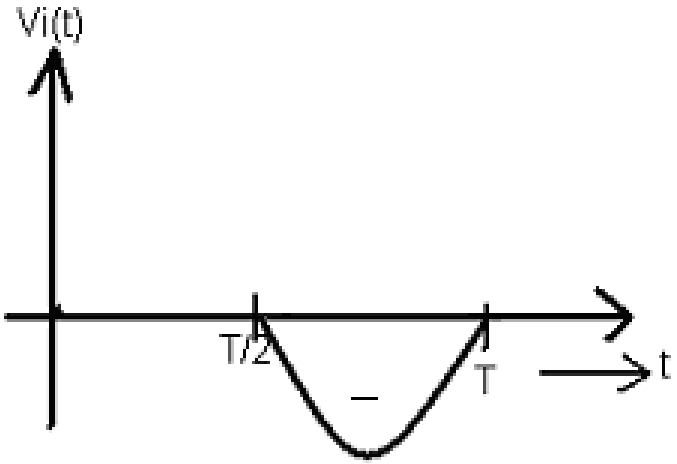


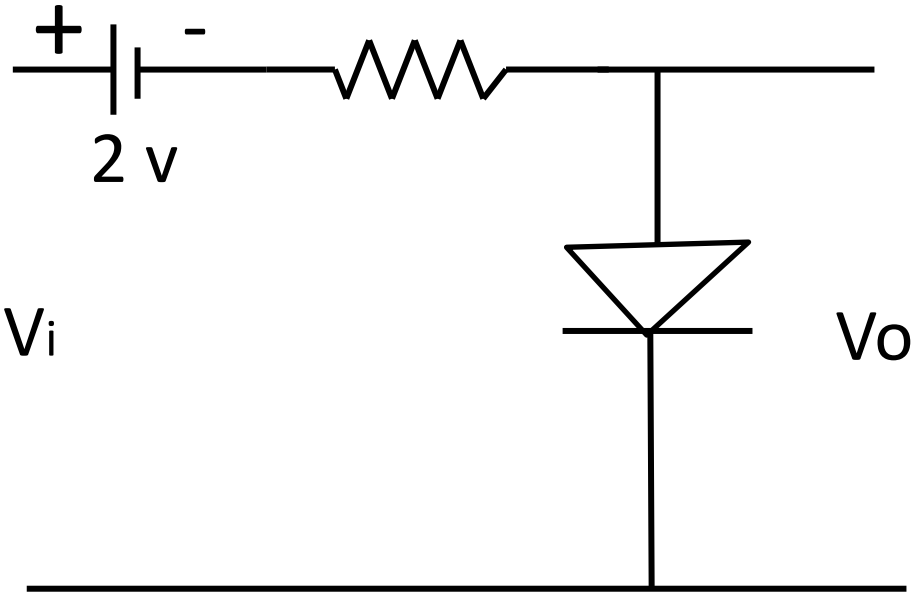


Diode is forward biased.

So Vo = V_D

For -ve half cycle





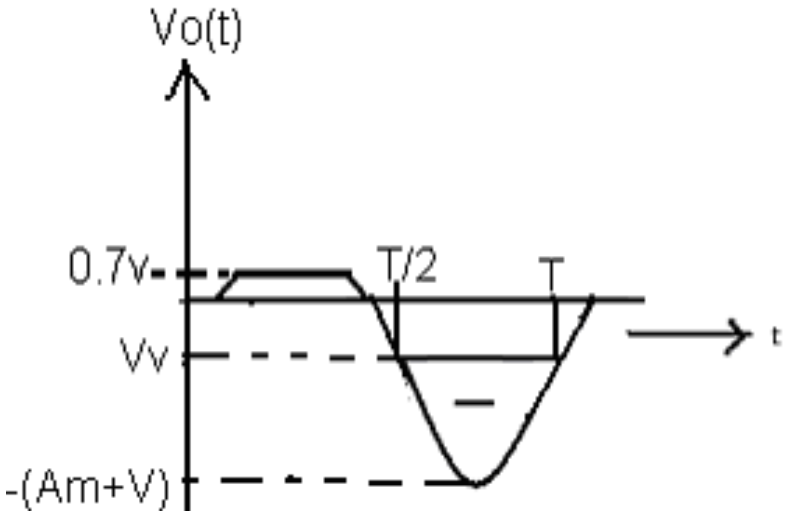
Diode is reverse biased.

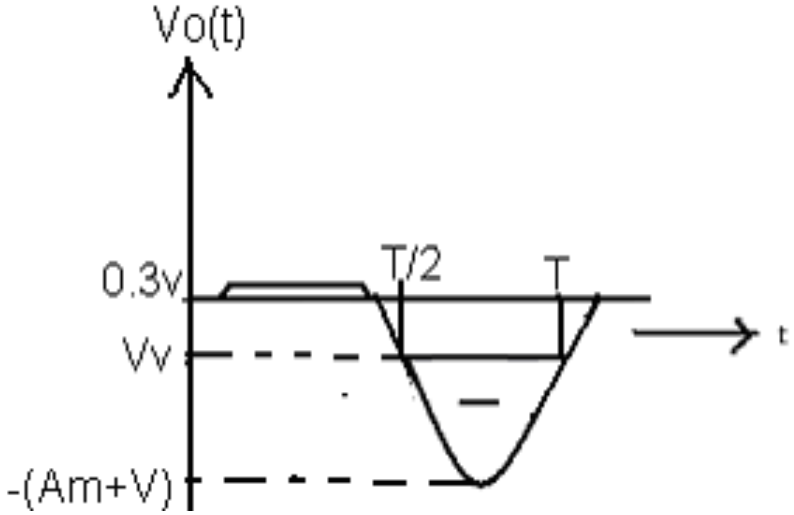
By KVL,

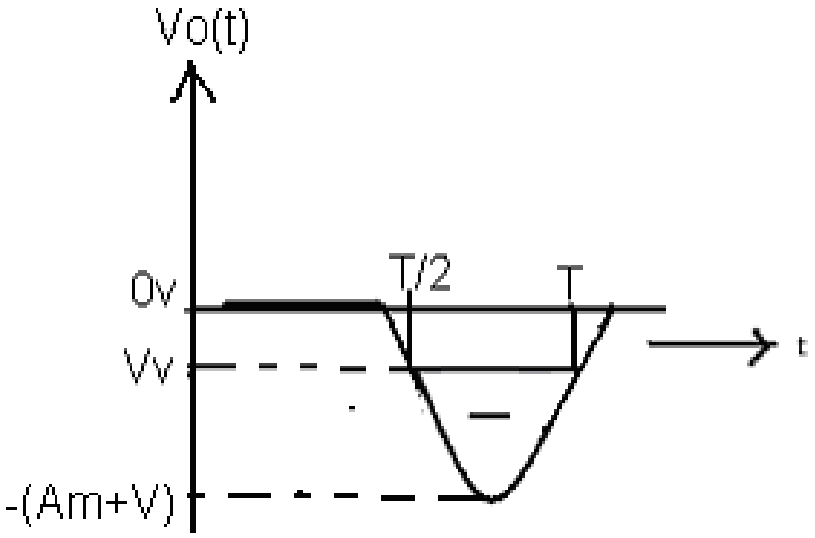
$2v + Vi + Vo = 0$

$\Rightarrow Vo = -(2v + Vi)$

The net output for the given input signal



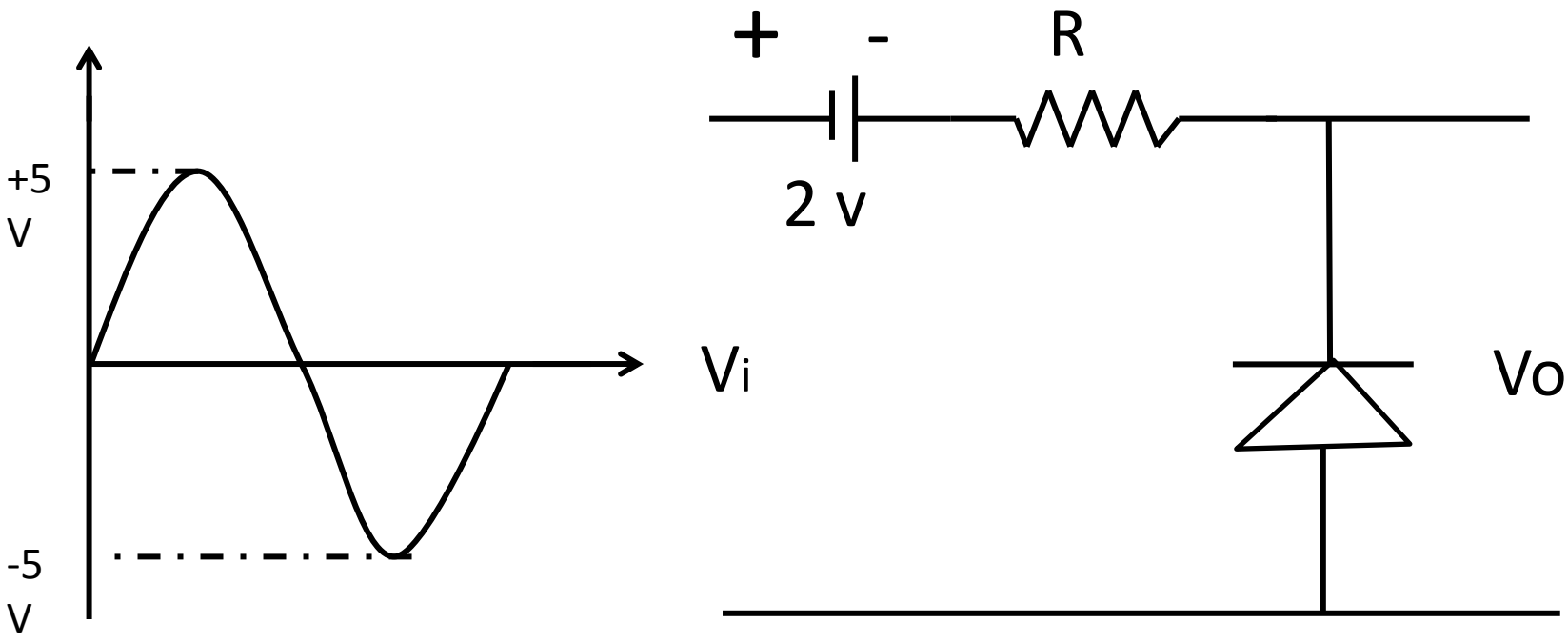




PRACTICE

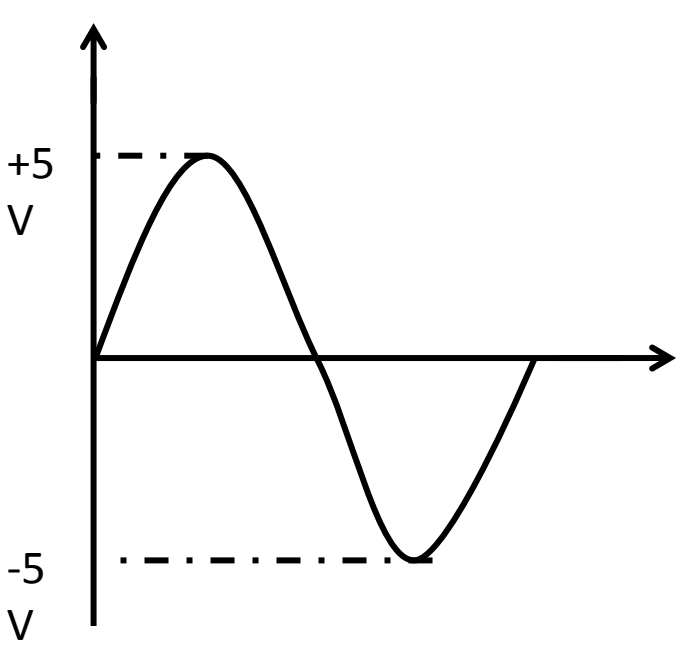
1. Biased clippers:

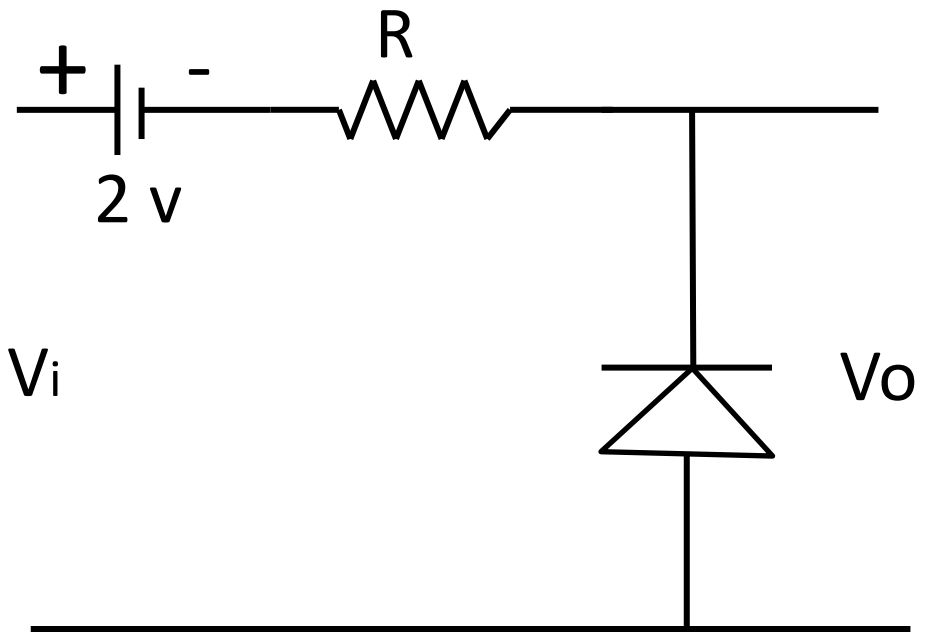
Draw the output waveform for the given circuit assuming the diode as Si type, Ge type & Ideal.



2. Biased clippers:

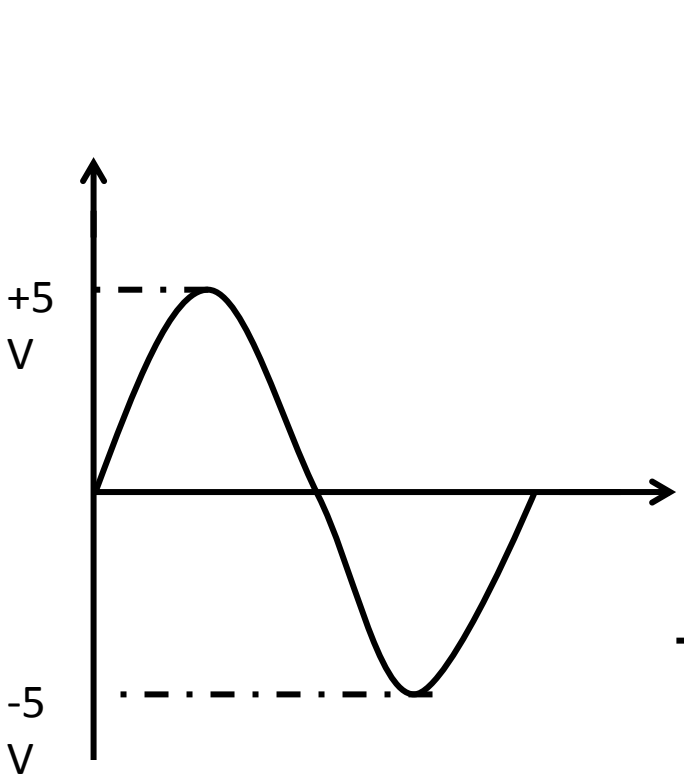
Draw the output waveform for the given circuit assuming the diode as Si type, Ge type & Ideal.

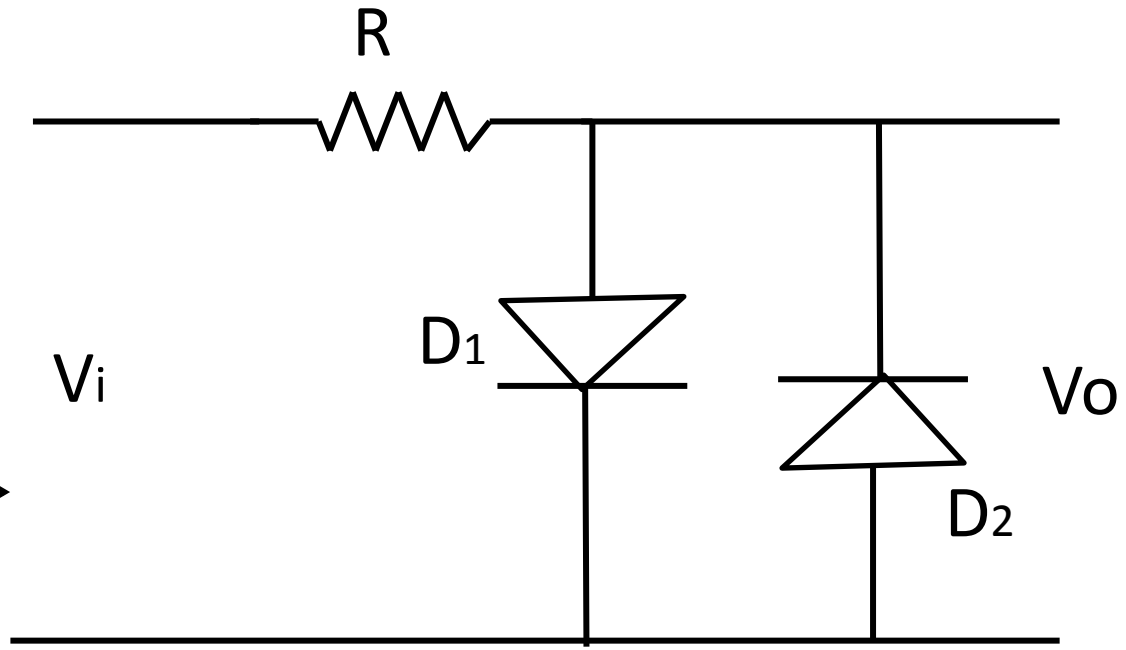




3.Combination clippers:

Draw the output waveform for the given circuit assuming the diode as Si type, Ge type & Ideal.





4.Combination clippers:

Draw the output waveform for the given circuit assuming the diode as Si type, Ge type & Ideal.